
# NATIONAL STRATEGY ON MICROELECTRONICS RESEARCH

*A Report by the*

SUBCOMMITTEE ON MICROELECTRONICS LEADERSHIP

COMMITTEE ON HOMELAND AND NATIONAL SECURITY

*of the*

NATIONAL SCIENCE AND TECHNOLOGY COUNCIL

March 2024

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## About the Subcommittee on Microelectronics Leadership

The Subcommittee on Microelectronics Leadership (SML) of the NSTC was established pursuant to Section 9906 of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Public Law 116-283), Title XCIX. SML coordinates activities across the Executive Branch of the federal government related to U.S. leadership and competitiveness in microelectronics technology and innovation. SML is also helping to coordinate Executive Branch implementation of the CHIPS Act of 2022 (Division A of Public Law 117-167) with the broader whole-of-government effort to grow the nation's semiconductor manufacturing base and accelerate microelectronics research and development (R&D), including activities by agencies not funded specifically to perform additional semiconductor/microelectronics R&D under the CHIPS Act of 2022 (e.g., the National Science Foundation, the Department of Energy, and the Defense Advanced Research Projects Agency).

## About this document

This document is the National Strategy on Microelectronics Research called for in Section 9906 of Public Law (P.L.) 116-283, Title XCIX. This strategy identifies four goals to guide agency efforts in microelectronics research to (a) accelerate the domestic development and production of microelectronics and strengthen the domestic microelectronics workforce; and (b) ensure that the United States remains a global leader in the field of microelectronics R&D. In addition to input from the many agencies represented on SML, it reflects extensive consultation with the Industrial Advisory Committee established under P.L. 116-283 as well as other stakeholders from industry, non-governmental organizations, and academia.

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## Table of Contents

## Abbreviations and Acronyms[1]

| | |
|---|---|
| **2D** | two-dimensional |
| **3D** | three-dimensional |
| **3DHI** | 3D heterogeneous integration |
| **ADK** | assembly design kit |
| **AI** | artificial intelligence |
| **CHIPS** | Creating Helpful Incentives to Produce Semiconductors (abbreviation for P.L. 116-283, Title XCIX, and Division A of P.L. 117-167) |
| **CMOS** | complementary metal-oxide-semiconductor |
| **DARPA** | Defense Advanced Research Projects Agency |
| **DTCO** | design-technology co-optimization |
| **EDA** | electronic design automation |
| **ENIAC** | Electronic Numerical Integrator and Computer |
| **FFRDC** | Federally Funded Research and Development Center |
| **FLOPS** | floating-point operations per second |
| **HBCU(s)** | Historically Black Colleges and Universities |
| **IP** | intellectual property |
| **KSAs** | knowledge, skills, and abilities |
| **MEMS** | microelectromechanical systems |
| **MGI** | Materials Genome Initiative |
| **ML** | machine learning |
| **MSI** | minority-serving institution |
| **NASA** | National Aeronautics and Space Administration |
| **NGMM** | Next-Generation Microsystems Manufacturing (DARPA program) |
| **nm** | nanometer |
| **NNCI** | National Nanotechnology Coordinated Infrastructure (NSF program) |
| **NNI** | National Nanotechnology Initiative |
| **NSTC** | National Semiconductor Technology Center (also, National Science and Technology Council) |
| **OECD** | Organisation for Economic Co-operation and Development |
| **OSTP** | Office of Science and Technology Policy |
| **PDK** | process design kit |
| **RFI** | Request for Information |
| **R&D** | research and development |
| **Si** | silicon |
| **STCO** | system technology co-optimization |
| **STEM** | science, technology, engineering, and mathematics |
| **TCCU** | Tribally Controlled Colleges and Universities |

[1] See the Subcommittee on Microelectronics Leadership roster (pp. i-ii) for spelling out of acronyms of participating agency names.

## Executive Summary

Decades ago, American innovation sparked the research advances that led to the semiconductor industry of today. This industry is global, underpins everything from health to communications, and is essential for the economy and security of the United States. The significant investments made possible by the bipartisan CHIPS Acts provide opportunities to reinvigorate domestic manufacturing in this critical sector, and strengthen the microelectronics research and development (R&D) innovation ecosystem that can advance the American competitive position for the future.

This National Strategy on Microelectronics Research presents goals, key needs, and actions required over the next five years to realize these opportunities. This strategy provides the framework for federal departments and agencies, academia, industry, nonprofits, and international allies and partners to address key needs and build out the microelectronics research and development infrastructure to support the future advances that will shape the semiconductor field.

As highlighted throughout this report, the significant CHIPS R&D investments underway must be fully leveraged and coordinated with the broad portfolio of ongoing programs, activities, and resources that contribute to microelectronics research and development. Over the next five years, the White House and federal departments and agencies will work together to advance four interconnected goals:

- Enable and Accelerate Research Advances for Future Generations of Microelectronics
- Support, Build, and Bridge Microelectronics Infrastructure from Research to Manufacturing
- Grow and Sustain the Technical Workforce for the Microelectronics Research and Development to Manufacturing Ecosystem
- Create a Vibrant Microelectronics Innovation Ecosystem to Accelerate the Transition of Research and Development to U.S. Industry

The first goal focuses on key research needs in several areas that are required to accelerate the advances required for future generations of microelectronic systems. Research areas include materials that can provide new capabilities; circuit design, simulation, and emulation tools; new architectures and associated hardware designs; processes and metrology for advanced packaging and heterogeneous integration; hardware integrity and security; and manufacturing tools and processes to enable transition of new innovations into production.

These research areas require access to specialized tools and equipment. The second goal is focused on supporting, expanding, and connecting the research infrastructure from small-scale material and device-level fabrication and characterization through prototyping, large-scale fabrication, and advanced assembly, packaging, and testing. The required tools include both software (including design tools) and commercial-scale production and metrology hardware.

Expansion of the domestic semiconductor industry will also expand opportunities for good-paying jobs across the country. Goal three identifies efforts to support learners and educators in the development of the technical workforce required from research through manufacturing.

Finally, goal four is focused on the entire R&D landscape and presents strategies and actions to create a vibrant microelectronics innovation ecosystem to accelerate the transition of new advances into commercial applications. Key efforts not only support actions at each stage of the microelectronics technology development pathway, but also connect the various networks and activities to build a virtuous cycle of microelectronics innovation.

These four goals will be pursued in the context of the global nature of the semiconductor industry. As is the case with the semiconductor manufacturing supply chain, research facilities and talent that support the microelectronics innovation ecosystem are located all over the world. International collaboration, trade, and diplomacy are important tools to leverage efforts and resources, promote talent flow and research collaboration, and ensure secure supply chains.

Implementation of this strategy will result in a vibrant innovation ecosystem that accelerates new research breakthroughs, supports the transition of these advances to manufacturing, and provides good-paying jobs to people all across America. A fully built-out and well-connected microelectronics research infrastructure will provide the foundation for researchers to advance their breakthroughs and lead to a virtuous innovation cycle. Nurturing and supporting microelectronics innovation will help secure future leadership in the semiconductor industry for the security and prosperity of the United States and its allies and partners.

## Introduction

The microelectronics[2] revolution has transformed society. Nearly all aspects of modern life are now dependent on semiconductor technology, including communications, computing, entertainment, health care, energy, and transportation. As a result, microelectronics are essential to the economic and national security of the United States. Rapid innovation in the semiconductor industry has been fueled for decades by research and development (R&D) investments in hardware and software by the federal government and the private sector.[3]

The intense race to continually increase the performance and functionality of microelectronics, while maintaining or reducing cost and power requirements, has driven the fabrication of ever smaller and more densely integrated microelectronic components. This miniaturization has required continuous breakthroughs in materials, tools, and design that have enabled key structures within the components to have dimensions as small as a few atoms in size. While reductions in feature size have led to dramatic increases in digital information storage and processing capacity, there have also been many significant advances in analog and non-silicon technologies that are critical for communications, power, and sensing. The required advances in manufacturing have been enabled by significant investments not only in R&D, but also in developing the manufacturing and metrology equipment and the associated fabrication ("fabs") and packaging facilities required to make advanced integrated circuits and components. The complexity and cost of manufacturing at this scale—establishing a leading-edge[4] silicon fab complex now costs tens of billions of dollars[5]—has contributed to significant consolidation in the industry. Today, only three corporations in the world are competing to manufacture the latest generations of advanced logic devices.[6]

In June 2021, the White House released *Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth*, a report on critical supply chains, including the semiconductor manufacturing and advanced packaging supply chain.[7] The report noted that although U.S.-headquartered semiconductor companies accounted for nearly half of worldwide revenue, the share of global semiconductor manufacturing conducted domestically had dropped from 37% in 1990 to 12%, and the U.S. share of packaging had fallen to 3%.[8] As discussed in the report, modern

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2 Microelectronics in this context refers to integrated electronic devices and systems generally manufactured using semiconductor-based materials and related processing (i.e., in a semiconductor fabrication manufacturing facility, or "fab"). Such devices and systems include analog and digital electronics, power electronics, optics and photonics, and micromechanics for memory, processing, sensing, and communications applications.

3 The semiconductor industry refers to the manufacturing sector including design and production of products consisting of semiconductor-based electronic devices and integrated circuits, along with advanced packaging and power electronics.

4 "Leading-edge" refers to the most miniaturized or "scaled" digital computing and memory technology—currently denoted the "3 nm node"—with new, smaller nodes being produced every two to three years.

5 For example, see, *TSMC looks to double down on U.S. chip factories as talks in Europe falter*, https://www.globalbankingandfinance.com/exclusive-tsmc-looks-to-double-down-on-u-s-chip-factories-as-talks-in-europe-falter; and *Intel: Upcoming U.S. Fab Will Be a Small City, to Cost $60 to $120 Billion,* https://www.tomshardware.com/news/intel-to-spend-up-to-120-billion-on-new-us-manufacturing-hub.

6 See, The Semiconductor Supply Chain: Assessing National Competitiveness, https://cset.georgetown.edu/wp-content/uploads/The-Semiconductor-Supply-Chain-Issue-Brief.pdf.

7 *Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth*, The White House, 2021, https://www.whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf. Note: This initial report did not include power electronics or other specialized semiconductors for clean energy applications such as photovoltaics (PVs), which were addressed in follow-on reports: https://www.energy.gov/policy/securing-americas-clean-energy-supply-chain.

8 The U.S. share of global assembly, test, and packaging is now estimated to be less than 2%: https://www.bis.doc.gov/index.php/documents/technology-evaluation/3402-section-9904-report-final-20231221/file.

microelectronics manufacturing is an incredibly complex and global process, involving hundreds of steps completed over several months, with many components using international expertise and facilities as they traverse the world several times. The report concluded that the public and private sectors need to act to increase domestic manufacturing capacity for critical goods, recruit and train a domestic workforce, invest in R&D, and work with America's allies and partners to collectively strengthen supply chain resilience.

***National Strategy on Microelectronics Research—Goals and Objectives***

***Goal 1. Enable and Accelerate Research Advances for Future Generations of Microelectronics***

- *1.1: Accelerate the research and development of materials that provide new capabilities or functional enhancements.*
- *1.2: Increase the capabilities of circuit design, simulation, and emulation tools.*
- *1.3: Develop a diverse array of robust processing architectures and associated hardware needed for future systems.*
- *1.4: Develop processes and metrology for advanced packaging and heterogeneous integration.*
- *1.5: Prioritize hardware integrity and security as an element in co-design strategies across the stack.*
- *1.6: Invest in R&D for manufacturing tools and processes needed to support transition of innovations into production-worthy fabrication processes.*

***Goal 2. Support, Build, and Bridge Microelectronics Infrastructure from Research to Manufacturing***

- *2.1: Support federated networks of device-scale R&D fabrication and characterization user facilities.*
- *2.2: Improve access for the academic and small-business research community to flexible design tools and wafer-scale fabrication resources.*
- *2.3: Facilitate research access to key functional materials.*
- *2.4: Expand access to advanced cyberinfrastructure for modeling and simulation.*
- *2.5: Support advanced research, development, and prototyping to bridge the lab-to-fab gap.*
- *2.6: Support advanced assembly, packaging, and testing.*

***Goal 3. Grow and Sustain the Technical Workforce for the Microelectronics R&D to Manufacturing Ecosystem***

- *3.1: Support learners and educators in and across science and technology disciplines relevant to microelectronics.*
- *3.2: Foster meaningful public engagement in microelectronics and raise awareness of career opportunities in the semiconductor industry.*
- *3.3: Prepare an inclusive current and future microelectronics workforce.*
- *3.4: Build and drive microelectronics research and innovation capacity.*

***Goal 4. Create a Vibrant Microelectronics Innovation Ecosystem to Accelerate the Transition of R&D to U.S. Industry***

- *4.1: Support, build, and bridge centers, public private partnerships, and consortia to deepen collaboration among various stakeholders in the microelectronics ecosystem.*
- *4.2: Engage with and leverage the CHIPS Industrial Advisory Committee.*
- *4.3: Motivate and align the microelectronics community on key technical challenges with R&D roadmaps and grand challenges.*
- *4.4: Facilitate academic, government, and industrial exchange to broaden understanding of needs and opportunities.*
- *4.5: Support entrepreneurship, start-ups, and early-stage businesses through targeted programs and investments.*

***Microelectronics have become essential for many aspects of everyday life.***

*Semiconductors are critical to U.S. economic and national security and have become essential to many aspects of everyday life. Examples depicted here include automotive, health care, aerospace, virtual reality, financial systems, e-commerce, space satellites, defense, energy, computing, agriculture, and telecommunications. As microelectronic devices have become pervasive, their key performance requirements have become increasingly diverse, necessitating a divergence from the traditional scaling in feature size exemplified by Moore's Law. For example, the requirements for satellite applications include proven technologies that are radiation hardened, supercomputers maximize performance and speed, but devices on the edge such as sensors may prioritize low power. These application-specific requirements are driving an increased diversification of microelectronics, which will be enabled and advanced by approaches such as heterogeneous integration and chiplets.*

Image credits: Adobe istock.

The White House supply chain report emphasized the importance of the semiconductor industry to the U.S. economy, which ranked fifth overall in U.S. export sales in 2022.[9] The federal government is also an important consumer of microelectronics, and it is critical that it has access to trusted and assured microelectronics for essential functions such as communications, navigation, sensing, critical infrastructure, public health, and national security. Microelectronics underpin a wide range of emerging technologies including quantum information sciences, artificial intelligence, advanced wireless networks (6G and beyond), safe and secure health care technologies, and clean-energy and energy-efficient technologies needed to address the climate crisis.[10]

[9] *State of the U.S. Semiconductor Industry*, Semiconductor Industry Association, 2023, https://www.semiconductors.org/wp-content/uploads/2023/07/SIA_State-of-Industry-Report_2023_Final_072723.pdf, p. 23

[10] *Climate change widespread, rapid, and intensifying, IPCC*, https://www.ipcc.ch/2021/08/09/ar6-wg1-20210809-pr

***ENIAC on a chip***

*To illustrate the significant changes in size and scale of computing technologies, students designed and built "ENIAC-on-a-chip" to celebrate the 50th anniversary of the first programmable, electronic, general-purpose digital computer called the Electronic Numerical Integrator and Computer (ENIAC).[11] ENIAC was designed under a U.S. Army R&D program and was completed in 1945. ENIAC contained over 18,000 vacuum tubes and was approximately 8 feet tall, 3 feet deep, 100 feet long, and weighed more than 30 tons. ENIAC was programmed by hand using cables and switches, as illustrated in the figure on the left. The image on the right depicts a chip that recreated ENIAC using 0.5 µm complementary metal-oxide-semiconductor (CMOS) technology in 1995, replacing the vacuum tubes with transistors. Using today's technology, the chip would be approximately 1,000 times smaller. With respect to performance, ENIAC could do about 500 floating-point operations per second (FLOPS) while the Frontier supercomputer at Oak Ridge National Laboratory can now do more than one quintillion (1,000,000,000,000,000,000) FLOPS.*

Image credits: Left—Alamy Stock Photo; Right—Trustees of the University of Pennsylvania, all rights reserved, 1998 (photo by Felice Macera).

It is because of the importance of this industry to the nation's economy and security that the bipartisan CHIPS Act of 2022 (Division A of the CHIPS and Science Act of 2022[12]) was enacted and appropriated more than $52 billion to grow the nation's semiconductor manufacturing base and accelerate microelectronics R&D. Moreover, several recent reports have emphasized the importance of the industry. For example, in a 2018 assessment, the Department of Defense (DOD) identified threats to the microelectronics supply chain as well as related R&D and manufacturing issues for multiple critical defense sectors.[13] In 2020–2023, the Congressional Research Service (CRS) examined the technical challenges facing the semiconductor industry, domestic and global supply chains, secure and trusted production of semiconductors for national security, and associated federal policies and research investments, along with possible legislation to address these challenges.[14] The Final Report of the

[11] https://www.seas.upenn.edu/~jan/eniacproj.html

[12] CHIPS Act of 2022 (Division A of Public Law 117-167), https://www.congress.gov/bill/117th-congress/house-bill/4346/text: https://www.congress.gov/bill/117th-congress/house-bill/4346

[13] *Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States*, DOD, 2018, https://media.defense.gov/2018/oct/05/2002048904/-1/-1/1/assessing-and-strengthening-the-manufacturing-and%20defense-industrial-base-and-supply-chain-resiliency.pdf

[14] See: *Semiconductors: U.S. Industry, Global Competition, and Federal Policy*, Congressional Research Service, 2020, https://crsreports.congress.gov/product/pdf/R/R46581; *Semiconductors, CHIPS for America, and Appropriations in the U.S. Innovation and Competition Act (S. 1260)*, Congressional Research Service, 2022, https://crsreports.congress.gov/product/pdf/IF/IF12016; *Semiconductors and the Semiconductor Industry*, https://crsreports.congress.gov/product/pdf/R/R47508; *Frequently Asked Questions: CHIPS Act of 2022 Provisions and*

National Security Commission on Artificial Intelligence (AI) identified domestically-located semiconductor fabs as a requirement to maintain the nation's leadership in AI.[15] Semiconductors and microelectronics were also identified as areas of particular importance to the national security of the United States in the updated Critical and Emerging Technologies List.[16]

***Just how small is a transistor?***

*The following images show the size of transistors compared to an ant. The diameter of the circle around the picture of the ant depicts 2 millimeters (mm), or 0.002 meters. The next image is a picture taken in a scanning electron microscope (SEM) of an ant's eye, about 150 micrometers (µm), or 0.00015 meters in diameter. The third image is a picture of a hair on the ant's eye. The circle is 20 µm across. The fourth picture is a close-up SEM image of the hair, showing grooves on the hair. The diameter is 1 µm (or one thousand nanometers [nm]). A cross-section of integrated circuit transistors is shown in the top electron microscope image, illustrating modern integrated circuit transistors fit into a groove of the hair on an ant's eye. The diameter of this image is just 50 nm.*

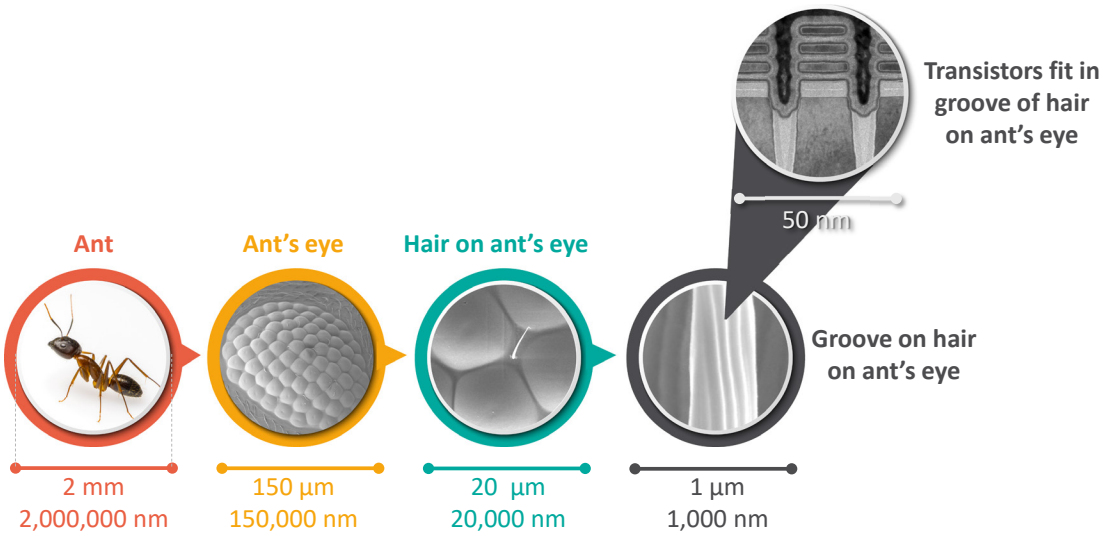



Image credits: Bottom images—National Institute of Standards and Technology (NIST); Upper right image—reprint courtesy of IBM Corporation ©.

Microelectronics R&D is essential to continue advancing technology and systems, and to realize the long-term goal of strengthening domestic manufacturing and mitigating supply chain risks. Additionally, input from federal Requests for Information (RFIs),[17] recommendations from the

*Implementation*, https://crsreports.congress.gov/product/pdf/R/R47523; *Semiconductors and the CHIPS Act: The Global Context*, Congressional Research Service, 2023, https://crsreports.congress.gov/product/pdf/R/R47558.

[15] See Chapter 13 of *Final Report*, National Security Commission on Artificial Intelligence, 2021, https://www.nscai.gov/wp-content/uploads/2021/03/Full-Report-Digital-1.pdf.

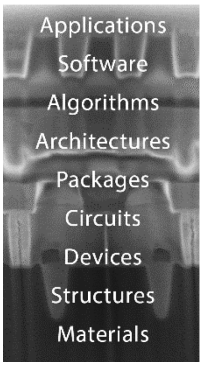
[16] https://www.whitehouse.gov/wp-content/uploads/2022/02/02-2022-Critical-and-Emerging-Technologies-List-Update.pdf

[17] Relevant RFIs include *Current and Future Workforce Needs to Support a Strong Domestic Semiconductor Industry*, NIST, DOC, 2018, https://www.federalregister.gov/documents/2018/07/16/2018-15077/current-and-future-workforce-needs-to-support-a-strong-domestic-semiconductor-industry; *National Nanotechnology Initiative Strategic Planning*, OSTP, 2020, https://www.federalregister.gov/documents/2020/10/13/2020-22556/request-for-information-national-nanotechnology-initiative-strategic-planning; *Microelectronics R&D Facility Capabilities for Prototyping,* DOD, 2020, https://sam.gov/opp/eaf0eb36b54542b28c6ee88252e9f4b0/view; *Basic Research Initiative for Microelectronics*, Office of Science, DOE, 2019, https://www.federalregister.gov/documents/2019/07/12/2019-14869/request-for-information-basic-

stakeholder community, and multiple other reports from the public and private sectors,[18,19] make it clear that a strong, innovative domestic R&D effort is vital to future U.S. competitiveness and security. Taken all together, a set of key R&D trends and opportunities emerge from these resources:

- **The diversity of devices and their applications continues to grow beyond conventional processors and memory**, requiring innovation throughout the generation, communication, storage, and processing of data across many scales and types of information systems.
- **Microelectronics technology is critical to fields beyond information technology**, with tremendous growth expected in areas such as power management, medical devices, and sensing.
- **A comprehensive approach to R&D across the "full stack" provides an opportunity to achieve performance, reliability, and security improvements in devices and systems**. Although much attention is focused on the design and scaling of foundational devices, there are also major challenges ahead for fabrication, metrology, testing, verification and validation, heterogeneous integration, and advanced packaging. Moreover, challenges are not limited to hardware: advances in devices, design and manufacturing, circuits, and systems integration require concomitant innovations across the computer architecture, software, and application layers.
- **Integrated design offers an approach to accelerate innovation**. In addition, it can ensure that critical system attributes are captured from the start and considered throughout the development cycle, including performance, reliability, energy efficiency, and security.
- **The U.S. microelectronics research ecosystem continues to excel at basic and early-stage applied research**, but additional investment in domestic infrastructure, a renewed emphasis on manufacturing science and engineering, and an agile workforce are needed to efficiently transition innovations to industry.
- **Affordable and rapid access to design and prototyping capabilities will increasingly enable domestic innovations to transition more rapidly from R&D into manufacturing**.

***What is "the stack"?***




*Throughout this report, the "stack" or "full stack" refers to the full range of science and technology elements required to make up a complete microelectronics system shown in the figure at right, from the most basic levels of hardware (e.g., materials and circuits) all the way through the high-level software and the applications where it will be used. (Background image is a cross section of a state-of-the-art chip. Image credit: NIST.)*

research-initiative-for-microelectronics; and *Draft National Strategy on Microelectronics Research*, OSTP, 2022, https://www.federalregister.gov/documents/2022/09/15/2022-19935/request-for-information-draft-national-strategy-on-microelectronics-research.

[18] Public sector reports include *Basic Research Needs for Microelectronics*, DOE, 2018, https://www.osti.gov/biblio/1545772; *Semiconductor Foundry Access by U.S. Academic Researchers in Micro- and Nano- Circuits and Systems*, NSF, 2021, https://nsfedaworkshop.nd.edu/assets/429148/nsf20_foundry_meeting_report.pdf; and *Report of the first DOE\AMO Workshop on Semiconductor RDD&D for Energy Efficiency*, DOE, 2021, https://www.energy.gov/eere/amo/articles/amo-semiconductor-workshop-integrated-sensor-systems-report. In addition, summaries of other AMO workshops in this series can be found at https://www.energy.gov/eere/ammto/resource-library.

[19] Private sector reports include, for example, *Semiconductor Research Opportunities: An Industry Vision and Guide*, Semiconductor Industry Association (SIA), 2017, https://www.semiconductors.org/wp-content/uploads/2018/06/SIA-SRC-Vision-Report-3.30.17.pdf; *Chipping In:,* SIA, 2021, https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf; *The Decadal Plan for Semiconductors*, Semiconductor Research Corporation, 2021, https://www.src.org/about/decadal-plan, and *An Analysis of the North American Semiconductor and Advanced Packaging Ecosystem,* IPC, 2021, https://emails.ipc.org/links/IPCadvpack-ecosystem-report-final.pdf.

Capabilities are needed from the device scale to the wafer scale, both near or at leading-edge process nodes, as well as at the more mature nodes important for analog and non-silicon technologies. Students and researchers need access to these capabilities for experiential workforce training.

- **Access to well-prepared talent is a significant challenge across the entire value chain** and will require both short-term and long-term solutions. Welcoming pathways are needed to make the United States a magnet for outstanding foreign talent in high-demand fields. Improvements in both curriculum and outreach are needed to develop and expand the equitable, inclusive, and diverse domestic science, technology, engineering, and mathematics (STEM) talent pool to support microelectronics R&D and the semiconductor industry.
- **Strong engagement with allies and partners is required to ensure the success of the entire innovation ecosystem**. The semiconductor industry is global; no nation can bring together the technology, supply chains, and expertise to support leading-edge R&D and manufacturing alone. Tech diplomacy will be an important tool to engage allies and partners.
- **Improving the energy efficiency of microelectronics is increasingly essential for sustainability**. Rapid growth in microelectronics use and the simultaneous slowing of energy efficiency improvements are creating new economic and environmental risks. To reduce these risks, microelectronics R&D investments must include a focus on energy efficiency and on full-life-cycle sustainability, including reducing the use of materials that are scarce or hazardous to the environment.
- **Safeguarding intellectual property is essential to ensure that U.S. industry captures economic benefit to sustain private R&D investments.** Key intellectual property developed by and within the United States must be protected, while also improving the ability to appropriately share information among collaborative efforts. Applied research is intended to provide technical discriminators giving microelectronics manufacturers a strategic advantage in the marketplace. Safeguards (i.e., cybersecurity, intellectual property enforcement, etc.) must be implemented and effectively enforced to ensure that key innovations are not inadvertently or inappropriately infringed upon.

These trends and opportunities have informed the goals, needs, and strategies presented in this document to accelerate the pace of innovation and translation through collaborative research, access to advanced infrastructure, and a culture of co-design across the microelectronics R&D enterprise. Attention must focus on developing and sustaining a vibrant and connected microelectronics ecosystem to ensure U.S. leadership in this important area.

## The Microelectronics Innovation Ecosystem

The microelectronics innovation ecosystem is complex and extremely capital-, knowledge-, and R&D-intensive.[20] Industry consolidation has imposed limits on the associated R&D ecosystem. With worldwide manufacturing of leading-edge microelectronics now dependent on only a handful of companies, the opportunity for researchers to exploit advanced processes is limited. Researchers in academia, government, and industry who do not require high-volume production have limited access to the capabilities needed for advancing the R&D frontier, significantly constraining their ability to develop and transition innovations to leading-edge manufacturing. Limited access to leading-edge

[20] For example, see *Measuring distortions in international markets: The semiconductor value chain,* OECD, 2019, https://www.oecd-ilibrary.org/trade/measuring-distortions-in-international-markets_8fe4491d-en; and *Strengthening the Global Semiconductor Supply Chain in an Uncertain Era*, Boston Consulting Group and the Semiconductor Industry Association, 2021, https://www.semiconductors.org/strengthening-the-global-semiconductor-supply-chain-in-an-uncertain-era.

capabilities also restricts opportunities to provide experiential training for workforce development. CHIPS Act investments aim to address these issues.

Beyond the leading edge of current CMOS technology, the microelectronics industry is facing profound changes associated with the accelerated pace of innovation and an explosion in the diversity of technologies emerging from academia, Department of Energy (DOE) National Laboratories and other Federally Funded Research and Development Centers (FFRDCs), nonprofit laboratories, government facilities, and companies small and large. Effective pathways for transitioning new research advances into applications need to be established and strengthened to ensure that the United States captures the benefits from R&D investments and that key intellectual property (IP) is available for domestic manufacturing. Additionally, as new challenges are identified in manufacturing, these technical needs must be communicated back to the research community.

As part of the national R&D ecosystem, over 20 federal agencies fund R&D, with the nature of the activities determined by the mission of each agency.[21] The Department of Commerce (DOC), National Aeronautics and Space Administration (NASA), National Science Foundation (NSF), Department of Homeland Security (DHS), Department of Health and Human Services (HHS), DOD, DOE, and other federal agencies support both intramural R&D (conducted within government facilities and DOE National Laboratories) and extramural R&D (conducted by academia, industry, and other organizations through grants, contracts, and other agreements). The wide span of R&D activities supported by federal research funding requires that IP developed is protected from unintentional, forced, or coerced technology transfer. Agencies also support workforce development across all educational levels through a variety of mechanisms, including support for formal and informal learning, internships, and fellowships; curriculum development; and coordinated efforts to broaden participation in STEM. While each agency has mission-oriented priorities determining the focus of its microelectronics-related research, as discussed below and throughout this strategy, there are multiple interagency mechanisms in place to coordinate R&D priorities and programs and to ensure that the outcomes of research are shared for mutual benefit.

Within the microelectronics innovation ecosystem, an important element of federal funding is support for infrastructure along the technology development pathway. For early-stage research, many facilities exist in academic institutions, government facilities, and DOE National Laboratories and other FFRDCs, particularly for the fabrication and characterization of materials and devices. Another area of federal investment is in cyber infrastructure, including modeling, simulation, and data. Several user facility networks connected to the National Nanotechnology Initiative (NNI)[22] provide researchers from academia, industry, and government with access to suites of tools and scientific expertise that support microelectronics R&D. These facilities have vastly broadened participation of researchers from small businesses and institutions that would not be able to purchase the equipment on their own. This has helped democratize innovation that requires specialized facilities and equipment, especially for semiconductor R&D and fabrication.

Once proofs of concepts at the device level are achieved, innovation often becomes hindered in the current U.S. ecosystem by a lack of access to the necessary advanced development capabilities. Investments in domestic materials supply, design, fabrication, and packaging capabilities are required to address this laboratory-to-fabrication (lab-to-fab) gap. Investments are required to enable and sustain advanced prototyping and scale-up of new devices and architectures, along with the associated manufacturing and metrology instrumentation, and in concert with the required design of software and

[21] See Research and Development chapter of *Analytical Perspectives: Budget of the U.S. Government, Fiscal Year 2024:* https://www.whitehouse.gov/wp-content/uploads/2023/03/ap_6_research_fy2024.pdf.

[22] https://www.nano.gov/userfacilities

applications. Moreover, access to these capabilities by both researchers and students will provide hands-on experiential training to expand the domestic microelectronics workforce.

The CHIPS for America Act of 2021[23] authorized multiple programs to help bridge this lab-to-fab gap, while the CHIPS Act of 2022[24] appropriated funding for the programs. Section 9903 of the CHIPS for America Act of 2021 authorizes DOD to establish a National Network for Microelectronics Research and Development to enable the lab-to-fab transition of microelectronics innovations in the United States. Section 9906 directs DOC to establish a National Semiconductor Technology Center to conduct research and prototyping of advanced semiconductor technologies; a microelectronics research program at NIST to conduct semiconductor metrology research and development; a National Advanced Packaging Manufacturing Program to strengthen semiconductor advanced test, assembly, and packaging capabilities; and up to three Manufacturing USA institutes focused on semiconductor manufacturing.

Within the broader U.S. R&D ecosystem, there are many regional innovation hubs around the country composed of industry clusters complemented by federally supported academic centers, often focused on specific technologies and/or local research strengths. These local hubs are valuable national resources, and ensuring that they are well coupled to other elements of the overall R&D ecosystem, including microelectronics, will strengthen the national innovation base.

The U.S. semiconductor industry invests heavily in R&D efforts, estimated to be nearly $60 billion in 2022.[25] To maintain their world-leading expenditures on R&D, U.S. companies must have access to foreign markets where they can compete and win based on superior technology. Trade policy must protect U.S. companies from discrimination in global markets. Collaboration and alignment with allies and partners will help address national security concerns and help U.S. companies hold their ground in the intense global competition for technology leadership.

The White House and federal departments and agencies recognize that openness is a foundation for R&D leadership and that international talent flow is critical to the success of the global enterprise.[26,27] However, as made clear in Guidance for Implementing National Security Presidential Memorandum 33 (NSPM-33),[28] the U.S. government and its partners must strengthen protections of R&D against foreign government interference and exploitation, diligently safeguarding intellectual capital and property. Protections may include improved, risk-based processes for evaluating research partnerships and proposed foreign investments; active participation of U.S. experts in international standards organizations; closer coordination with international partners on research security; and a campaign of outreach and education on the importance of this topic across the microelectronics R&D community.[29]

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[23] William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021, (Public Law 116-283), Title XCIX ("Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America") (herein "CHIPS for America Act of 2021")

[24] CHIPS Act of 2022 (Division A of Public Law 117-167), https://www.congress.gov/bill/117th-congress/house-bill/4346/text: https://www.congress.gov/bill/117th-congress/house-bill/4346

[25] *State of the U.S. Semiconductor Industry*, Semiconductor Industry Association, 2023, https://www.semiconductors.org/wp-content/uploads/2023/07/SIA_State-of-Industry-Report_2023_Final_072723.pdf, p. 21

[26] https://www.quantum.gov/wp-content/uploads/2021/10/2021_NSTC_ESIX_INTL_TALENT_QIS.pdf

[27] https://www.whitehouse.gov/briefing-room/statements-releases/2022/01/21/fact-sheet-biden-harris-administration-actions-to-attract-stem-talent-and-strengthen-our-economy-and-competitiveness/.

[28] Guidance For Implementing National Security Presidential Memorandum 33 (NSPM-33) On National Security Strategy For United States Government-Supported Research And Development, https://www.whitehouse.gov/wp-content/uploads/2022/01/010422-NSPM-33-Implementation-Guidance.pdf

[29] *United States Government National Standards Strategy for Critical and Emerging Technology*, White House, 2023, https://www.whitehouse.gov/wp-content/uploads/2023/05/US-Gov-National-Standards-Strategy-2023.pdf

## A Whole-of-Government Approach

Recognizing the critical role of microelectronics to our health, environment, economy, and national security, a whole-of-government effort is underway to sustain and advance global leadership by the United States and its allies in this important field. On August 25, 2022, President Biden released an Executive Order on the Implementation of the CHIPS Act of 2022 that identified implementation priorities and established the CHIPS Implementation Steering Council to coordinate policy development to ensure the effective implementation of the Act within the Executive Branch.[30] Co-chaired by the directors of the White House Office of Science and Technology Policy (OSTP), National Security Council (NSC), and National Economic Council (NEC), the steering council includes secretaries from the departments of State, Treasury, Defense, Commerce, Labor, and Energy; the Director of the Office of Management and Budget (OMB); the Administrator of the Small Business Administration; the Director of National Intelligence; the Assistant to the President for Domestic Policy; the Chair of the Council of Economic Advisers; the National Cyber Director; the Director of the National Science Foundation, and the Director of the National Institute of Standards and Technology. This council ensures awareness of ongoing efforts and investments across the government and coordinates policy development at the Cabinet level.

In accordance with Section 9906(a) of the William Mac Thornberry National Defense Authorization Act for Fiscal Year 2021, OSTP established the Subcommittee on Microelectronics Leadership (SML) under the National Science and Technology Council. The Subcommittee membership includes the Department of Commerce, the Department of Defense, the Department of Energy, the Department of Health and Human Services, the National Science Foundation, the State Department, the Department of Homeland Security, and the Office of the Director for National Intelligence. White House components represented include OSTP, OMB, NEC, NSC, and the Office of the U.S. Trade Representative.

Also pursuant to Section 9906(a), the Subcommittee is responsible for developing this National Strategy on Microelectronics Research; for coordinating microelectronics-related research, development, manufacturing, and supply chain security activities and budgets of federal agencies; and for ensuring that such activities are consistent with the strategy. As the body responsible for coordinating microelectronics efforts for the next decade, the SML is developing the structural framework and activities to best serve this role, including the establishment of working groups focused on education and workforce development, and on international engagement. The participating agencies are utilizing their respective authorities to advance R&D and promote policies to support U.S. industry, protect intellectual property, and ensure domestic access to secure microelectronics. Agencies are also collaboratively supporting activities to improve STEM education and increase participation in STEM fields, and to train and expand the microelectronics workforce at all levels. The federal government is engaging and collaborating with allies and partners to strengthen the global microelectronics innovation ecosystem and secure supply chains. Coordinated through the White House, these efforts will not only fuel new research advances to drive microelectronics innovation, but will also help these advances transition to manufacturing and provide good-paying jobs to people across all of America.

As detailed in the sections below, the White House and federal departments and agencies will work together and with academia, industry, nonprofits, and international allies and partners to fuel research advances for future generations of microelectronics; establish best practices to ensure efficient,

[30] https://www.whitehouse.gov/briefing-room/presidential-actions/2022/08/25/executive-order-on-the-implementation-of-the-chips-act-of-2022/

accountable R&D execution; support and connect the microelectronics research infrastructure; expand, train, and support a diverse workforce; and facilitate the rapid transition of R&D to industry.[31]

## Goal 1. Enable and Accelerate Research Advances for Future Generations of Microelectronics

R&D supported by the federal government has been instrumental in laying the foundation for advances in microelectronics and in educating the research and skilled technical workforce needed for design, manufacturing, and application development. The increasing diversity of microelectronics technology and pace of innovation, combined with the growing risks to the global manufacturing and supply chain, requires a renewed federal focus on R&D investment in ways that will alter these trajectories and ensure the future health, economic leadership, and security of the nation. Success requires strategies that engage all sectors of the R&D ecosystem and leverage education, workforce, manufacturing, trade, and regional economic development efforts and policies. Federal agencies, in collaboration with industry, academia, and partners and allies, must work together to accelerate the pace of innovation and translation through collaborative research, access to advanced infrastructure, and a culture of co-design across the microelectronics R&D enterprise.

The past six decades have seen incredible progress in computational power and energy efficiency, enabled in part by continued miniaturization (supported by concomitant advances in materials, design, metrology, and manufacturing). However, this trend in transistor scaling cannot continue indefinitely as the smallest device feature sizes approach the atomic scale. Furthermore, there are emerging applications that will require heterogeneous devices and materials. The semiconductor industry has therefore entered a period of rapid and profound change, and one in which performance advances can no longer be sustained solely by continued miniaturization of silicon-based devices.

For example:

- The explosion of data and the emergence of artificial intelligence enabled by machine learning (ML) is driving the development of “compute-in-memory” and other novel memory-intensive and memory-centric architectures that promise to overcome the “von Neumann bottleneck”—the energy inefficiency and high latency caused by shuttling data back and forth between separate memory and compute elements.
- As intrachip and interchip data rates have increased, photonic interconnects, previously only used in long-haul links over optical fiber, are being integrated with electronics in advanced packaging to move data efficiently.
- Advances in materials and devices are enabling ultra-high-frequency free-space communication using mm-wave and THz systems.
- Advanced photonics are poised to deliver dedicated artificial intelligence/machine learning (AI/ML) hardware that operates at low power and extraordinary speed.

[31] Many aspects of microelectronics R&D intersect with other initiatives and Biden-Harris Administration priorities, including the National Nanotechnology Initiative, the Future Advanced Computing Ecosystem (formerly the National Strategic Computing Initiative), the National Quantum Initiative, and the Networking and Information Technology Research and Development (NITRD) Program. SML is working with all of these efforts to ensure synergy and coordination.

***Dramatic progress in scaling of microelectronic devices since the first digital computers***

*This graph illustrates the change in the number of components on an integrated circuit, or chip, over time, along with some of the technological innovations that enabled the different waves of progress. For reference, the first programmable, electronic, general-purpose digital computer, ENIAC, built using vacuum tubes, is the first point in 1945. (See more about ENIAC in the call-out on p. 4.) The first transistor, made from germanium, was invented in 1947 and was approximately 1 cm long. The first silicon transistor came a few years later. The first silicon integrated circuit was demonstrated in late 1959. With the invention of the first metal-oxide-semiconductor field effect transistor (MOSFET) integrated circuit in the early 1960s, the number of components began to increase exponentially. Each time progress slowed, advances in manufacturing science, materials, and device design re-energized the field. In the first wave, shrinking the size of the transistor, the basic building block of these chips, led directly to dramatic increases in the number of components on a chip and dramatic reductions in the cost per transistor—the observation that formed the basis for Moore's Law. The original planar integrated circuit went from small-scale integration (SSI) to medium-scale integration (MSI) to large-scale integration (LSI) to very large-scale integration (VLSI). During the second wave, the introduction of new materials, including the transition from aluminum to copper interconnects, resulted in better speed, power, and reliability, and enabled further reduction in transistor size. The third wave began with the transition from planar to three dimensional (3D) transistors using fin field-effect transistors (FinFETs), resulting in additional performance gains and continued miniaturization. As the technologies for shrinking the size of the transistors, which are now only a few atoms across, reach their physical limits, new strategies are required. We are at the start of the "4th wave of microelectronics," leaving behind device scaling and entering into an age where higher performance will be driven by innovations in the integration of heterogeneous technologies and 3D devices. While efforts continue to decrease transistor size, new tools, manufacturing methods, and circuit architectures must be developed to deliver continued progress.*

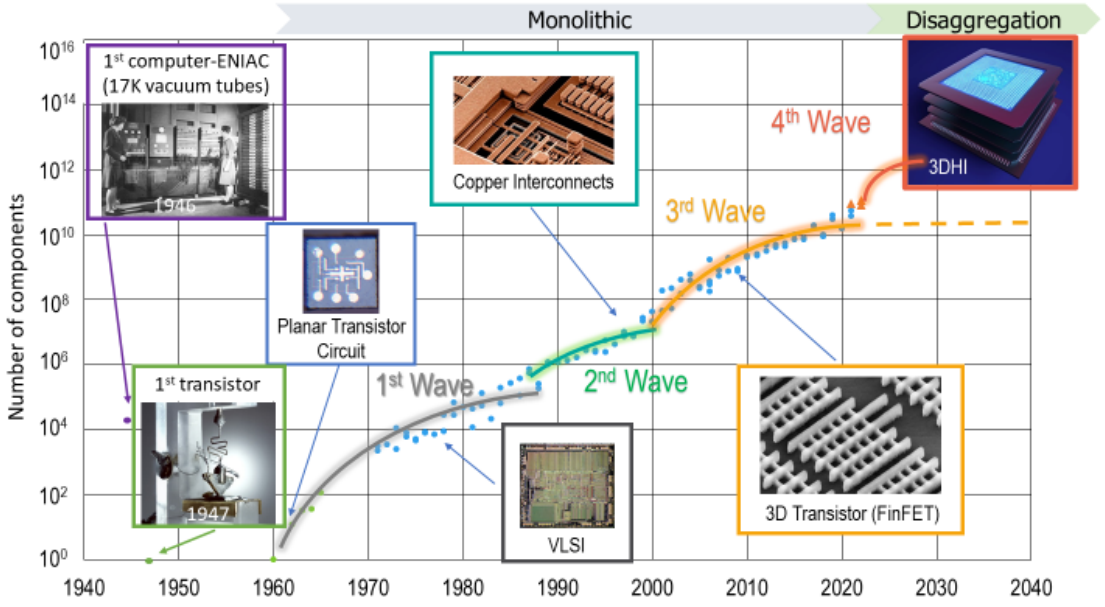



Image credit: Defense Advanced Research Projects Agency (DARPA).

- A revolution is underway in electronic design automation (EDA), including the application of AI/ML, cloud-based platforms, and design-technology co-optimization (DTCO) that will make it feasible for designers to create ever-more-complex integrated circuits, optimized for almost every conceivable application, faster and more reliably. These circuits will deliver tremendous gains in speed and efficiency and affect the performance of every information technology sector, from data centers to edge computing and the internet of things (IoT).
- Heterogeneous and domain-specific computing architectures that optimize performance for specific applications are being deployed to accelerate time-to-solution.
- Microelectromechanical systems (MEMS) are becoming increasingly sophisticated and powerful as they are integrated with processing and intelligence.
- Progress is being made in integrating semiconductor systems with biomolecular, biological, neuromorphic, and bio-inspired systems that may one day deliver unprecedented improvements in energy efficiency and other unique capabilities in computation, AI, robotics, sensing, and health care beyond the potential of either domain on its own.
- As the demands for different applications diverge, extreme reliability and operation at cryogenic temperatures, high temperatures, or low power will modify the standard metrics of power, performance, area, and cost driving the development of new devices, architectures, and algorithms.
- As electronics move towards more heterogeneous architectures, performance metrics become more complex. Heterogeneous integration—the science and technology of bringing disparate materials, devices, and circuits together to create highly functional, high-performance systems—is key to enabling continued progress. However, as more and more diverse components are integrated, the physical, electronic, optical, and software challenges of making them operate seamlessly together become more complex.
- Dramatic increases in system heterogeneity and complexity also call for R&D attention on design flows that prioritize security and reliability, and that integrate both formal and empirical verification and validation throughout the full design, fabrication, and manufacturing process.

As referenced in the introduction, there are calls to not only support the underlying science and engineering that shape and drive microelectronics, including computer science, computing architectures, physics, chemistry, and materials science, but also to widely embrace the principles of integrated design where these different aspects of research inform and guide each other synergistically, and with sustainable development in mind. Open communication between all levels of the stack is essential to ensure that end-use capabilities and requirements inform research, and that research breakthroughs are rapidly incorporated into development efforts. Such an integrated approach is the only way to guarantee that critical system attributes such as security, reliability, and radiation-hardness[32] are designed in from the start and considered throughout the development cycle. Lastly, with the projected increase in resources needed to produce, operate, and eventually recycle microelectronics systems, a comprehensive approach to estimating total lifetime energy consumption and cost will need input and expertise from across the entire supply chain to identify opportunities to develop more efficient architectures and processes.

[32] Some space, energy, and defense applications require electronics that must function when subjected to a range of radiation sources, including cosmic rays. Radiation-hardened microelectronics perform critical sensing and computational functions so that these devices work as intended in harsh environments.

***Integrated design***

*Integrated design refers to a constant bidirectional flow of information from the top to the bottom of the stack driven by applications. Linking end-user needs to R&D is essential for rapid, focused technological development and deployment of research and development to the market. The figure at right illustrates this bidirectional flow of information among the various levels of the stack: material-to-circuit physical models; materials and processes; architectures, devices, and circuits; heterogeneous integration and packaging; algorithms and software; and communications and networks.*

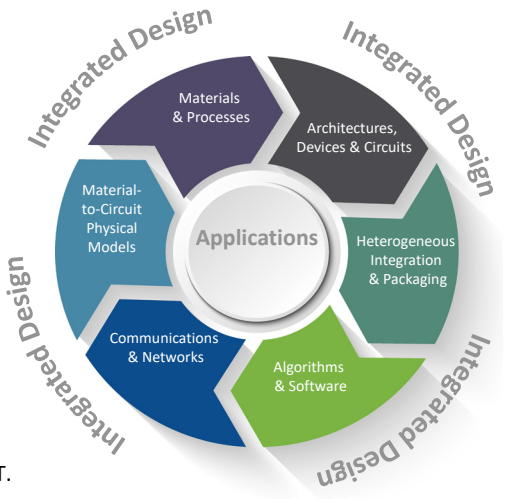



Image credit: NIST.

Future leadership in microelectronics requires industry to overcome significant challenges in device physics and fabrication. Deep innovation is therefore needed to identify and transition novel materials and devices from lab-to-fab to enable continued advances in functionality and performance. Successful establishment of a lab-to-fab pathway will require renewed focus on the intersection between fundamental science and manufacturing technologies. Satisfying the ever-increasing demand for storage, bandwidth, and processing power in information and computing technology (ICT) systems, along with the expected growth in the spectrum of applications beyond ICT, requires research and development from devices to systems, and from design to process technology. Central to this strategy is the need for access to design and fabrication facilities, including those equipped to incorporate unconventional materials and/or processes, often in heterogeneous combination with silicon (Si)-CMOS technologies. Innovations across all levels of the stack need to be fully exploited to enable further progress with complex scalable designs in leading-edge Si-CMOS.

Advances in characterization tools and techniques will also be needed to enable detailed and comprehensive investigations of new materials and designs, and to do so with unprecedented spatial resolution, sensitivity, bandwidth, and throughput. The increasing complexity of circuits and systems, including those operating with signals in and interacting across multiple physical domains, will require complementary, multimodal metrology tools as well as new modeling and simulation capabilities to measure performance and provide the data necessary to support EDA, DTCO, and system technology co-optimization (STCO). As the sophistication of these models grows, they will increasingly inform the development of manufacturing process improvements.

In addition to coordination across the hardware-software stack, coordination is required across the R&D community through synergistic flow of research results to achieve the best outcomes. University and small-business researchers must have access to design tools, fabrication facilities, and related infrastructure in which to test their ideas. Commercial fabrication facilities will benefit from working with early-stage testers of novel technology approaches. Likewise, industry R&D will benefit from the training of an advanced research workforce skilled in these areas and graduating from U.S. universities to join their corporate R&D efforts. An important aspect of this collaboration must be to establish and maintain effective research security measures to prevent R&D activities from creating unintended technology transfer.

Over the next five years, U.S. government R&D efforts will focus on the following objectives:

### 1.1: Accelerate the research and development of materials that provide new capabilities or functional enhancements.

Materials R&D is central to meeting emerging needs across all sectors and application areas. New and improved materials are required to meet goals in energy efficiency, information speed and bandwidth, novel computing architecture, and sustainable development. For example, emerging substrate materials such as silicon carbide (SiC), indium phosphide (InP), aluminum nitride (AlN), or diamond are under development. There are many promising new wide-bandgap, and ultra-wide-bandgap materials for applications in power electronics and radio-frequency electronics (6G and beyond), and while available, thin-film silicon nitride (SiN) and lithium niobate ($LiNbO_3$) materials need to be improved to advance photonic applications and next-generation wireless communication. New multiferroic and memristive materials are expanding the range of functions that nanoelectronic devices can provide. However, despite these many exciting breakthroughs, the introduction of new materials into complex microelectronics process flows typically takes decades of effort and billions of dollars to go from proof-of-concept to manufacturing. To enable novel and emerging materials to fulfil their potential, new approaches are needed to dramatically reduce the time and cost to deployment.

Coordination among entities in the semiconductor materials and associated research ecosystem, including national labs, private sector companies, and consortia, will provide pathways to deployment of advanced materials for devices, interconnects, circuits, and systems. Frameworks like the Materials Innovation Infrastructure developed as part of the Materials Genome Initiative (MGI)[33] can play an important role in organizing the materials community around grand challenges in developing new capabilities or functional enhancements for microelectronics.

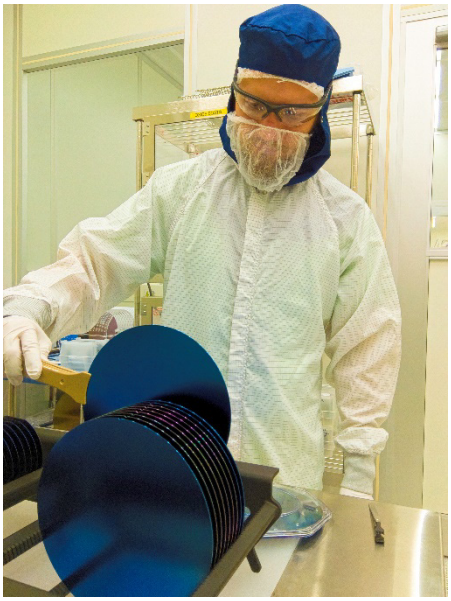
Elements of advanced materials R&D needed to support new capabilities include:

- Focused research on emerging organic and inorganic materials including two-dimensional (2D) materials; materials exhibiting quantum effects/properties; wide-bandgap and ultra-wide-bandgap materials for energy-efficient electronics and use in extreme environments; materials optimized for high-bandwidth interconnects; materials for ultra-high-frequency operation (optical, electrical, and electromechanical); materials that enable non-von Neumann architectures; and biotic-abiotic hybrid systems.
- Exploration of materials that can be seamlessly integrated into existing process flows, and that can, for example, add functionality into the back-end-of-line (BEOL) to improve performance and allow for greater 3D integration.
- Increased efforts to improve existing bulk substrate materials and to accelerate the development and deployment of new ones.
- Unified semiconductor materials data infrastructure to facilitate knowledge sharing and accelerate innovation.
- New modeling, characterization, and metrology methods to allow the rapid, precise, and accurate determination of *all* of the parameters relevant to real-world applications.
- R&D efforts to accelerate the development of manufacturable synthesis processes and production-worthy tools for new and emerging materials.
- New measurements and standards to ensure purity, physical properties, and provenance to accelerate materials research and development.[34]

[33] NSTC Materials Genome Initiative Strategic Plan, 2021, https://www.mgi.gov/sites/default/files/documents/MGI-2021-Strategic-Plan.pdf

[34] *Strategic Opportunities for U.S. Semiconductor Manufacturing*, NIST, 2022, https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf, p.6

- Research to improve sustainability and circularity (reuse, recycling) in processing, fabrication, and supply chains through the full lifecycle, including more eco-friendly materials and extraction processes, and wider use of earth-abundant elements that reduce supply-chain vulnerabilities.
- Access to fabrication facilities equipped to incorporate unconventional materials and/or processes, possibly in heterogeneous combination with Si-CMOS technologies.
- Creation of new focused facilities to prove out and scale up processes for novel and unconventional materials.



Silicon wafers being loaded into a low-pressure chemical vapor deposition (LPCVD) furnace. Image credit: NIST.

### 1.2: Increase the capabilities of circuit design, simulation, and emulation tools.

Circuit design, simulation, and emulation tools applicable to new materials, devices, circuits, and architectures are essential to continued innovation and device scaling.

Strategic approaches to improve capabilities of digital tools include efforts to:

- Create, develop, and make widely available tools that can facilitate the design, modeling, simulation, and exploration of new forms of computing architectures and computing processors—both digital and analog/mixed signal; support designs using advanced packaging; and incorporate objectives including size, weight, power, cost, safety, and security.
- Further the integration of AI and ML, together with physics-based methods, in EDA tools to support the design and development of innovative circuit and system architectures.[35]
- Develop high-level synthesis tools and EDA systems and flows, integrated with simulation and optimization capabilities, with shorter learning curves to lower barriers to entry for integrated circuit designers.
- Improve materials and device validation methods and advance measurements of material, component, and circuit properties, in order to generate robust, statistical parameters needed to increase the fidelity of EDA tools.
- Improve DTCO and STCO methodologies and platforms to enable full-stack co-optimization.
- Advance the development of formal and end-to-end validation methods, including device-relevant materials data and input information, to overcome bottlenecks in circuit and system design and simulation to manage increasingly complex and heterogeneous systems.

### 1.3: Develop a diverse array of robust processing architectures and associated hardware needed for future systems.

The rapid growth and utilization of advanced computing resources for machine learning, augmented reality/virtual reality (AR/VR), image/signal processing, etc., have created performance and energy demands that are pushing the boundaries of state-of-the-art Si-CMOS designs. Non-von Neumann computing architectures, such as neuromorphic, memory-centric, deep learning, asynchronous

[35] *NSF Workshop on Micro/Nano Circuits and Systems Design and Design Automation: Challenges and Opportunities*, University of Notre Dame, 2021, https://nsfedaworkshop.nd.edu/assets/432289/nsf20_eda_workshop_report.pdf

computing, hybrid, and designs harnessing quantum effects, will be increasingly useful in a wide range of commercial and national security applications. In addition to systems based on standard Si-CMOS, new approaches employing cryogenic CMOS, analog/mixed-signal technologies, photonics, spintronics, and quantum devices are rapidly emerging. Making the most of this diverse array of processing architectures and device types requires innovations across the entire stack.

Key research and development needs include development of:

- Increased understanding of the algorithms, programming models, and compilers required for optimal performance of these architectures.
- Hardware, software, and standards-focused efforts to enhance device programmability and programmability abstraction.
- Manufacturing and design capabilities optimized to produce these novel processing architectures.
- Novel architectures in addition to new integrated circuit designs that enable the optimal integration of non-von Neumann components with traditional computing architectures.
- AI and ML approaches to address the challenges associated with the expected high data rates and large data volumes generated by heterogeneously integrated logic-memory devices.
- Quantum information science research, including quantum computing, quantum networking, and quantum sensing, which will demand a wide range of new systems design approaches in addition to advanced fabrication capabilities and exotic materials.[36]
- Quantum support technologies, such as cryogenic electronics and photonics, to interface with quantum systems.
- Energy-efficient processing architectures for large networks of sensors to extract and distill information, including sensor technologies, analog processing architectures, and extreme distributed edge computing using both classical and bio-inspired approaches.
- Design flows and architectures for sensing, signal processing, and computing applications in extreme environments.
- Circuit innovations beyond high-performance computing to address needs in energy, health care, transportation, and communications.

### 1.4: Develop processes and metrology for advanced packaging and heterogeneous integration.

Heterogeneous integration, which includes the integration of several distinct technologies (e.g., Si-CMOS, MEMS, III-V mixed signal, and photonics) that are themselves the result of integrating multiple systems, will be a critical driver of future innovation in microelectronics. Examples can include integration on single chips, multiple chips, or chiplets[37] on substrates, using a variety of approaches, such as 2.5D and 3D stacking, high-density redistribution, optical packaging and test, fan-out, hybrid bonding, advanced interposers, high-density solder bumps, copper interconnects, and vias. Success in heterogeneous integration leads to better yields, lower costs, greater functionality, re-use of IP enabling accelerated design iterations and customization, and improved energy efficiency. Integration is critical across application spaces that range from high-performance computing to health care to positioning, navigation, and timing. Heterogeneous integration and the advanced packaging technologies that make it possible are now growing faster than traditional packaging. This growth

[36] Coordinated under the National Quantum Initiative, see https://www.quantum.gov.

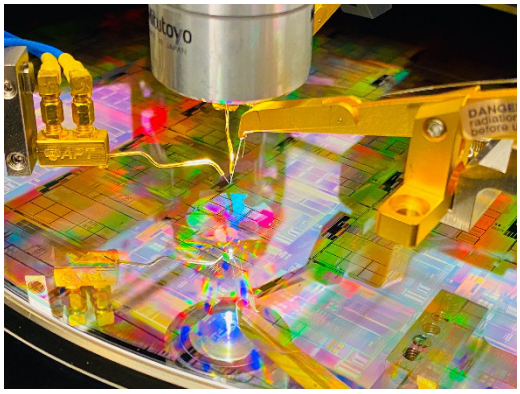
[37] The term “chiplet” refers to an integrated circuit unit with a specific purpose or function that can be combined with other units (chiplets) in a modular approach to design systems.

presents the United States with a rare opportunity to establish a lead in a critical area, despite the dominance of overseas assembly and test facilities in conventional packaging.

Successfully securing U.S. leadership in advanced packaging and reaping the benefits of heterogeneous integration will require addressing many interlinked research challenges, including materials, manufacturing processes, energy, cost, yield, and validated modeling.

Key research challenges include:

- New materials for substrates, encapsulation/molding, and die-to-die interconnects to expand the available design space, and for which collaboration and partnerships with materials suppliers will be essential.
- Advances in areas such as mechatronics, machine vision, and robotics to support the development of cost-effective, automated, agile systems for both high-volume and high-mix packaging and assembly.
- Innovative interconnect technologies to increase energy efficiency and density.
- New, high-speed methods to inspect components prior to assembly and to monitor interfaces during assembly to reduce defective components or defects in interfaces between components.
- Enhanced tool metrology and inspection capabilities, including novel optical sources and high-speed detectors over wavelengths from infrared to x-ray.



Integrated photonic devices in a probe station undergoing simultaneous optical and electronic measurement. Image credit: NIST.

- New metrology that spans multiple length scales (2D and 3D) and physical properties to address unique measurement challenges imposed by emerging heterogeneous integration and advanced packaging processes and technologies.
- Improved physics-based modeling of the thermal, mechanical, and electromagnetic behavior of the complete system and development of new, high-resolution methods to measure these behaviors to validate model accuracy and system performance.
- Integrated design tools and methods to ensure that circuits, architectures, and packages are co-designed to maximize system performance and IP re-use.

### 1.5: Prioritize hardware integrity and security as an element in co-design strategies across the stack.

In the face of threats from nation-state and criminal adversaries, the potential for the insertion of malicious alterations into components ranging from circuits to software, combined with the need to prepare for encryption and data security in a post-quantum-computing world, make it essential that integrity and cybersecurity be a foundational component of system design.[38,39] There are many attack

[38] Cybersecurity R&D challenges and goals for hardware and software are described in *Federal Cybersecurity Research and Development Strategic Plan*, OSTP, 2023, https://www.whitehouse.gov/ostp/news-updates/2023/12/31/federal-cybersecurity-research-and-development-strategic-plan/.

[39] https://www.whitehouse.gov/briefing-room/statements-releases/2022/05/04/national-security-memorandum-on-promoting-united-states-leadership-in-quantum-computing-while-mitigating-risks-to-vulnerable-cryptographic-systems/

vectors that must be mitigated, including side-channel, reverse-engineering, malicious hardware, and supply-chain manipulation. In recent years, cybersecurity threats have evolved from attacks focused high in the software stack to progressively lower levels of the computational hierarchy, down to the chip level. In addition to improving security, advances are needed across the stack to support enhanced privacy—the ability of individuals and organizations to control who has access to and control over their data and to what extent their data can be associated with them. Co-design of hardware with software is needed to meet these challenges in ways that provide maximum protection while minimizing the impact on system performance.[40] The design process must allow for iteration between hardware, software, and security/privacy constraints. To meet economic and national security needs, as well as maintain privacy, security must be incorporated in co-design R&D as a constraint, and it must be assigned the same priority as power, performance, area, and cost.

Research needs to improve hardware integrity and security include development of:

- Accurate threat models to support the analysis of the cost-benefit tradeoffs of different security approaches.
- High-level conceptual models of integrity and security (analogous to abstraction layers in computer science) to help the various disciplines in the co-design community communicate and collaborate more effectively.
- New automation and support structures to enable applications to be built on secure systems and to support the universal adoption of new applications.
- Co-design centers of excellence, in which security is a primary design constraint within each of the hardware focus areas.
- New methods to protect data and reduce the need to trust hardware, such as homomorphic encryption, encrypted memory systems, secure computation, sequestered encryption, and multi-party computation.
- Methods to ensure the provenance and integrity of integrated circuit IP.
- Standard test articles, methods, and analysis for evaluating and benchmarking measurement performance to promote measurement reproducibility between different organizations.[41]
- High-throughput measurement and inspection systems to enable verification of circuit hardware.

### 1.6: Invest in R&D for manufacturing tools and processes needed to support transition of innovations into production-worthy fabrication processes.

As R&D delivers new materials and devices, research is required to also develop the manufacturing tools and processes to enable the mass production of these new technologies. While important manufacturing technology advances will continue at micrometer scales, much that is cutting edge is already and will continue to be at the nanometer scale—even at the atomic scale for some features. To meet the demand for enhanced device performance and energy efficiency, the corresponding development of manufacturing processes, tools, and metrology with unprecedented precision is required. So-called "ultra-precision manufacturing" (UPM) is the next step in a long history of manufacturing at ever-smaller scales.[42] The need for ultra-precision also presents an opportunity to take advantage of material properties that are unique to the nanometer scale, such as tunneling or

[40] See, for example, D. Dangwai et al., *SoK: Opportunities for Software-Hardware-Security Codesign for Next Generation Secure Computing*, 2021, https://arxiv.org/abs/2105.00378.

[41] *5G Hardware Supply Chain Security Through Physical Measurements*, NIST, 2022, https://doi.org/10.6028/NIST.SP.1278

[42] See for example, N. Taniguchi, Current status in, and future trends of, ultraprecision machining and ultrafine materials processing, *CIRP Annals*, 32(2) (1983): 573–582, https://doi.org/10.1016/S0007-8506(07)60185-1.

magnetic and spin interactions, to realize powerful new functionalities. Novel fabrication methods will be effective only if they can be scaled to achieve commercial volumes. Advanced manufacturing R&D to scale up processes and tools to meet the demands of manufacturing is therefore essential.[43] Conversely, there are also opportunities to develop more agile manufacturing approaches that enable cost-effective, high-mix, low-volume production to support increasingly diverse commercial and defense needs. In addition, there are significant opportunities to advance manufacturing technology at larger feature sizes to improve yields, reduce process and device variation, and enable cost-competitive, resource-efficient domestic manufacturing.

Key R&D needs for new tools and processes include:

- Ultra-precision characterization, advanced lithography, and metrology tools, alongside improved quality control, including accurate reference structures at the sub-10-nm scale.
- Novel approaches to patterning, both subtractive and additive, that support emerging needs such as 3D architectures, large-area substrates, and high-mix, low-volume manufacturing of circuits and packages.
- Improvements in processes such as area-selective atomic-layer deposition and etching to support reduced feature sizes and more complex device geometries.
- High-throughput experimentation and modelling methods, coupled with new capabilities in optical, electron, and scanning probe microscopy inspection tools to improve speed, throughput, yield, precision, and accuracy.
- Hybrid metrology methods that combine data from multiple measurement tools integrated with new ML methods to utilize the data and enable process optimization.
- Integrated AI/ML/physics-based models capable of digesting a fab's worth of real-time process data for advanced predictive analytics to measure and improve yield and enable fab virtualization in semiconductor and microelectronics manufacturing.
- Further development and use of *in situ* metrology to accelerate the integration of real-time process control and reduce process variability—a key driver of costly *ex situ* metrology. Progress in this area requires advances in the integration of multimodal measurements, software integration, and tool development.
- Rapid, high-resolution, non-destructive techniques for characterizing defects and impurities and correlating them with performance and reliability.
- Physical properties characterization for surfaces, buried features, interfaces, and devices with increased resolution, sensitivity, accuracy, and throughput.
- Application of first-principles materials research with high-performance computing to develop accurate materials-process interaction models.
- Advances in the application of digital twins to enable the accurate modeling and rapid iteration and convergence of manufacturing process flows.
- Improvements in energy and resource efficiency, and use of environmentally benign chemistry[44] in manufacturing processes.

[43] DOE Workshop report on Ultra-precise control for ultra-efficient devices: https://www.energy.gov/sites/default/files/2022-02/AMO%20Semiconductor%20Workshop%20II%20Report%20FINAL_compliant_02-08-2022.pdf

[44] https://www.whitehouse.gov/wp-content/uploads/2023/08/NSTC-JCEIPH-SCST-Sustainable-Chemistry-Federal-Landscape-Report-to-Congress.pdf

## Goal 2. Support, Build, and Bridge Microelectronics Infrastructure from Research to Manufacturing

As emphasized throughout this strategy, microelectronics R&D is extremely infrastructure-intensive, and access to the appropriate facilities and associated expertise is necessary at every development stage—from early-stage research through manufacturing. Furthermore, the resources for each stage must be connected to ensure that new innovations can rapidly progress along the technology development pathway. Historically, the United States has not had centralized, open-access facilities for microelectronics R&D that are equipped with the design and fabrication tools, testing, and expertise relevant to a manufacturing environment for leading-edge technologies, limiting opportunities for researchers to advance their innovations. Recognizing this gap in the ecosystem, Congress authorized and appropriated resources for several programs in the CHIPS Acts to help establish facilities that support domestic research maturation and access to advanced prototyping capabilities using manufacturing-relevant equipment. Additionally, the continued diversification of microelectronics to best address specific use cases results in a complex set of needs across the various R&D stakeholders. Researchers require straightforward access to facilities in the United States equipped with fabrication tools, testing capabilities, and skilled technicians to maintain and operate them. This infrastructure support empowers researchers to demonstrate the potential of new devices, interconnects, circuits, systems, and fabrication processes in a leading-edge (or near-leading-edge) manufacturing environment. A well-coordinated constellation of facilities with state-of-the-art equipment, design tools, and skilled technicians will also be essential for advancing leadership in heterogeneous integration.

The semiconductor R&D infrastructure exists across a continuum, supporting activities ranging from the exploration of new materials to the implementation of new system architectures. The incredible complexity of modern semiconductor and microelectronic systems is best managed by enabling each level in the stack to judiciously abstract and inform the key features of neighboring levels as part of a co-design approach with bidirectional information flows. Material characteristics are abstracted into device models, device behaviors are incorporated into circuit models, circuits into architectures, and so on up to applications. Likewise, application and software characteristics inform architectures, which guide circuit designs and so on down the stack.

As the R&D focus moves up the stack, the infrastructure must be aligned to ensure a continuous path for scientific and technological developments made at each level to inform those at the next, and ultimately to feed into commercial design and manufacturing. At the lowest level of the stack, maximum flexibility is required of facilities to accelerate the research and development of new materials that will enable breakthrough performance. As these materials are identified, they must be made available to the research community to integrate into devices to determine whether the anticipated performance benefits can be realized. Further up the stack, facility flexibility is less important compared to the existence of reliable and robust fabrication processes that enable repeatable and reliable measurements of device performance. At the circuit level, access to documented and supported process design kit (PDK) modules and foundational circuit IP, e.g., standard cell libraries, complemented by robust testing and characterization capabilities, are essential. At the package level, adaptable integration and characterization of monolithic and system-in-package designs, including advanced chiplet capabilities, are needed to support small- and medium-scale prototyping. Creating such a full-spectrum R&D ecosystem will require supporting and expanding cost-effective access to the infrastructure needed for innovation. This infrastructure comprises three critical components: hardware and software tools, data and data sharing infrastructure, and expertise to make

the best use of the tools and data. Affordable and timely access to these tools and data is also an essential prerequisite for training and maintaining the expertise of the research and manufacturing workforce.

The infrastructure needed to support the R&D continuum ranges from facilities for the early-stage development of materials, structures, devices, fabrication processes, and metrology and characterization tools, to access to leading-edge prototyping facilities using standardized processes. The CHIPS Acts investments are intended to bridge the gap between early-stage R&D and prototype, enabling experimentation with new materials, processes, and metrology. Collaboration mechanisms across departments and agencies are needed to facilitate the transition of work from one facility to the next as users' technologies mature and capabilities evolve.

It is important to note that while several programs are highlighted under the following objectives in support of the microelectronics research infrastructure (goal 2), they also play a critical role in advancing research to help secure technical leadership (goal 1), educating and training the future workforce (goal 3), and helping to connect the broader ecosystem (goal 4).

Federal efforts over the next five years will address the following objectives:

### 2.1: Support federated networks of device-scale R&D fabrication and characterization user facilities.

The support of new concepts for electronic, photonic, and micromechanical devices that advance both "More-Moore" and "More-Than-Moore" solutions[45] requires increasingly complex and costly characterization and fabrication tools and facilities. Semiconductor materials synthesis and characterization, and device fabrication and measurement, involve multiple steps using different tool sets. Researchers working in microelectronics need access to user facilities equipped with complete suites of fabrication and characterization tools that require constant capital investments to remain current. In addition to the instrumentation, effective user facilities require expert staff to maximize the operation of specialized tools, and to train new users, which helps lower the barrier to access and provides an important role in education and workforce development.

Fortunately, the microelectronics R&D community can build upon the foundation of existing facilities, including the user facilities established as part of the NNI.[46] User facilities and other shared research infrastructure located across the country provide access to advanced laboratories, equipment, and expertise to researchers from government, industry, and academia. Supported by multiple federal agencies, many of these infrastructure centers facilitate microelectronics-relevant R&D by providing access to clean rooms, characterization tools, materials science and synthesis laboratories, and modeling and simulation tools. In addition to providing access for research activities, these centers also serve as a powerful training and workforce development engine. For example, the NSF-funded National Nanotechnology Coordinated Infrastructure (NNCI) is a network of 16 sites across the country that involves 29 universities and other partner organizations and provides access to user facilities with fabrication and characterization tools. In addition to providing researchers from government, industry, and academia with access to over 2,200 individual tools in 71 distinct facilities, the NNCI network

[45] More-Moore refers to advances in CMOS transistor scaling, and More-than-Moore refers to incorporating devices with functionality that does not necessarily scale like Moore's Law, such as radio-frequency, photonic, and MEMS devices.

[46] These facilities include the NSF-funded National Nanotechnology Coordinated Infrastructure, based in universities across the country, the DOE Nanoscale Science Research Centers, co-located with other facilities in DOE National Laboratories, and the DOC/NIST Center for Nanoscale Science and Technology NanoFab and facilities being set up in support of the National Quantum Initiative, including the DOE National QIS Centers and NSF Q-AMASE program.

supports expert staff to assist researchers, and a suite of education, training, and outreach efforts. As the fourth iteration of NSF's user facilities focused largely on nanoelectronics, these facilities have serviced tens of thousands of researchers and helped train generations of students. Furthermore, access to the costly specialized equipment necessary for microelectronics research provides opportunities for students, faculty, and researchers from institutions or small businesses unable to purchase and house similar facilities on site, broadening participation and expanding the research community. In addition to the NNCI and other major university centers, the U.S. government provides access to National Laboratory facilities through DOE's five Nanoscale Science Research Centers (NSRCs) and the NIST Center for Nanoscale Science and Technology (CNST) NanoFab. The five NSRCs are DOE's premier user centers for interdisciplinary research at the nanoscale, serving as the basis for a national program that encompasses new science, new tools, and new computing capabilities. These laboratories contain clean rooms, nanofabrication resources, one-of-a-kind signature instruments, and other instruments not generally available except at major user facilities. The NIST NanoFab provides access to an extensive commercial, state-of-the-art tool set, including advanced capabilities for lithography, thin-film deposition, and nanostructure characterization, and a full-time technical support staff. Finally, other shared infrastructure such as characterization laboratories, computational and modeling resources, light and neutron sources, and manufacturing institutes have a role to play in developing future materials, processes, designs, standards, and workforce.

Researchers using an electron microscope. Image credit: NIST.

Key needs for the R&D fabrication and characterization facilities include:

- A gap analysis of current facilities followed by efforts to address capability gaps within existing facilities and establish new capabilities where needed to comprehensively address the needs of different areas and levels in the stack.
- A regularly updated searchable public registry of shared research resources that enables researchers to easily identify the programs and centers that best align with their needs.
- Support for advanced manufacturing technologies capable of incorporating emerging low-dimensional nanomaterials and nanodevices and other "More-Than-Moore" solutions into designs, along with circuits manufactured using mature and state-of-the-art techniques for both small- and medium-scale prototyping.
- Agreements with international entities in allied and partner countries as necessary to provide U.S.-based researchers with access to cutting-edge manufacturing facilities to bridge current domestic gaps.
- Funding models, using impact metrics primarily focused on meeting the needs of a broad and diverse user base, that enable facilities to acquire sufficient state-of-the-art tools to build critical mass in their focus area(s), support expert facility technical staff to guide and assist users, and afford ongoing recapitalization as needed to maintain both state-of-the-art and state-of-the-practice capabilities.
- Success metrics and funding mechanisms that incentivize training and education, including support for travel to centers for researchers who are in geographically disadvantaged locations.
- Reduced barriers to facility access including through outreach to the research community, affordable operating costs/fees, and simple, equitable access models, including improved

implementation of remote operation technologies to further extend the geographic reach of every facility and promote equity of access.
- FAIR (findable, accessible, interoperable, and reusable) data management systems to maximize access by the research community to information generated in the facilities.

### 2.2: Improve access for the academic and small-business research community to flexible design tools and wafer-scale fabrication resources.

Currently, the costs of design tools, notably PDKs, assembly design kits (ADKs), and EDA, combined with the costs of foundry fabrication runs, can be prohibitive for small-business and academic research communities, as well as for efforts at government facilities, DOE National Laboratories and other FFRDCs, and nonprofit laboratories. In addition, there is no well-established pathway for a wafer fabricated at a foundry, particularly at mid-flow, to be further processed in a more flexible research facility. The CHIPS Acts investments will help address this domestic gap between device-scale R&D and advanced prototyping, through investments in infrastructure complemented by new public-private partnerships. These efforts aim to provide efficient, affordable access to a network of shared resources for wafer-scale R&D, and to develop a chiplet R&D ecosystem.

Key needs to improve access to design tools and fabrication resources include:
- Flexible and affordable models, including potential open-sourcing capabilities for mature nodes, that expand the availability of advanced PDKs, standard cell libraries, and certain IP (i.e., memory controllers, cores, etc.) for domestic researchers while protecting commercial IP and proprietary information.
- Broader partnerships with EDA vendors to make design tools, including high-level synthesis tools, available to more university and small-business researchers at significantly reduced cost, and to accelerate the development of domain-specific EDA capabilities when needed. The DARPA Toolbox Initiative[47] and the DOD Rapid Assured Microelectronics Prototypes (RAMP)[48] efforts are examples of facilitating access to design tools and proven IP for the R&D community. Where possible, programs should promote the standardization of PDKs used in R&D to increase interoperability across design and manufacturing vendors.
- Accessible design tools and tool environments for both mature and emerging technologies, including secure cloud-based solutions, that can ensure capture and rigorous protection of IP, enable determination of IP provenance and rights, and respect export controls and other legal and regulatory boundaries.
- Standardized licensing agreements and non-disclosure agreements to minimize barriers to IP sharing and reduce cycle times for innovation.
- Access to high-performance computing resources required for modeling and simulation needed to support the evaluation of circuit performance prior to incurring prototyping costs.
- Increased multi-project wafer capacity at fabrication facilities, supplemented by equitable access to smaller-scale manufacturing capabilities, to reduce cost and design-test cycle times, for both integrated circuit and advanced packaging/heterogeneous integration, and to expand access and accelerate innovation.

[47] DARPA Toolbox Initiative: https://www.darpa.mil/work-with-us/darpa-toolbox-initiative
[48] RAMP program: https://www.cto.mil/ramp-project/

- A library and supply of standard "plug-and-play" chiplets with standard interfaces, and open-source reference implementations of those interfaces.
- Creation of and access to advanced packaging research facilities to accelerate innovation in advanced packaging, heterogeneous integration, and the development of a chiplet ecosystem.

### 2.3: Facilitate research access to key functional materials.

The microelectronics industry would not be possible without a supply of ultra-pure and nearly defect-free materials and isotopes. Development of new electronic, magnetic, and photonic devices is likewise dependent upon the supply of appropriate functional materials. Several of these novel materials are of intense interest to the R&D community and are being actively developed at the device, circuit, and system level in applications ranging from machine learning accelerators to quantum networks. These materials include III-V semiconductors (as well as quantum dot and quantum well materials made from them), thin-film lithium niobate, silicon carbide on insulator, diamond, and a host of multiferroics and piezoelectrics. However, many of these materials are only available from overseas suppliers. Other materials can be obtained domestically, but often only from a single university laboratory with limited capacity to supply external research groups and sometimes with inconsistent quality. Efforts to strengthen the domestic ecosystem may provide opportunities to support material suppliers and encourage the development of new material processes that would thereby reduce acquisition costs for researchers.

Strategies to ensure a robust and high-quality domestic supply of functional materials to accelerate the pace of device development and integration research include:

- Working with and utilizing U.S.-based materials suppliers to ensure that domestic capacity is maintained and expanded. Efforts include ensuring that the necessary institutional knowledge and expertise to support manufacturing continues to be developed and captured domestically.
- Supporting U.S.-based research institutions at the forefront of materials development to enable the dedicated staff required to expand the capacity to supply domestic researchers with their novel materials. Focused research grants requiring industrial participation could be used to build collaborations to develop the materials supply and transfer research expertise to the commercial sector.
- Investing in traditional and innovative methods, including MGI approaches, to shorten the path from the demonstration of promising materials to the availability of substrate supplies, including bulk substrate synthesis and thin-film deposition/epitaxy, to provide substrate materials with high purity and low defect density at sufficient size and scale.

### 2.4: Expand access to advanced cyberinfrastructure for modeling and simulation.

Innovation at the limits of physics, manufacturing, and metrology requires that a solid understanding of circuit performance and manufacturing processes be demonstrated in digital simulation before investing in advanced prototyping or costly experimentation. Improved modeling and simulation tools that fully leverage high-level synthesis of hardware accelerators and simulations for circuits and systems are needed, especially those based on novel materials, devices, interconnects, and architectures integrated with CMOS. Similarly, comprehensive physics-based models, backed by rich physical data sets, are needed to model complex, interdependent manufacturing processes. Given the challenges of compute-data co-location, it is likely that generic cloud resources will be insufficient, and that cyberinfrastructure support tailored to the needs of microelectronics R&D will be needed.

Key actions to support access to cyberinfrastructure for modeling and simulation include:

- Providing access to leadership-class computing and other cyberinfrastructure, including at DOE National Laboratories, other FFRDCs, and NSF-funded facilities.
- Facilitating close coordination among users, system developers, and metrology and prototyping facilities to ensure the availability of high-quality data sets to enable the construction of accurate materials, process, device, and system models.
- Establishing close connections with physical infrastructure and its outputs to effectively support the entire R&D community and assist with technology transfer.

### 2.5: Support advanced research, development, and prototyping to bridge the lab-to-fab gap.

While there is a strong foundation of early-stage research infrastructure, as detailed in section 2.1, access to more advanced infrastructure has been particularly challenging in the U.S. ecosystem. The CHIPS Acts provide a unique opportunity to support and provide access to advanced prototyping resources that will provide critical domestic capabilities to accelerate the insertion of research innovations onto silicon wafers using leading-edge CMOS processes, as well as other critical materials and technologies, such as compound semiconductors for mixed-signal and power electronics. These efforts need to identify funding models, using impact metrics primarily focused on meeting user needs that enable facilities to acquire sufficient state-of-the-art tools, support technical staff to guide and assist users, and afford ongoing recapitalization as needed to maintain both state-of-the-art and state-of-the-practice capabilities. Providing access to well-maintained and tightly integrated resources will also maximize the opportunities for informal learning and collaboration between students, researchers, and industrial and government end users. Each of the programs discussed below will leverage existing capabilities and will expand capacity and develop new capabilities currently not available in the domestic ecosystem.

Section 9903(b) of the CHIPS for America Act calls for DOD to establish a National Network for Microelectronics Research and Development, which is referred to as the Microelectronics Commons or simply the Commons.[49] The Commons is a program that enables the development of microelectronics materials, processes, devices, and architectural designs that are focused on national defense needs. The Commons will address the need for processes, materials, devices, and architectures to be developed and quickly ported and re-characterized as they transition from research to small-volume prototyping in labs, and finally to fabrication prototypes that can demonstrate the volume and characteristics required to ensure reduced risk for manufacturing. At-scale prototyping is high-risk and expensive, and small and mid-size companies and universities have great difficulty bridging that laboratory to fabrication or “lab-to-fab” transition between research ideas and realization of those ideas into manufacturing. The Commons will leverage non-traditional defense innovators (e.g., startups and universities) and lower some of the existing barriers that hinder their ability to evolve laboratory prototypes to fabrication prototypes. The Commons is a network of regional “hubs” [50] with early- to mid-stage development capabilities and associated “cores” with later-stage capabilities. The cores will work closely with hubs to align their efforts with commercial processes to facilitate transition of technologies. Additional maturation will occur utilizing subsequent programs and resources. The Microelectronics Commons is focused in six technical areas important to national defense and

[49] https://microelectronicscommons.org/

[50] Initial awards were announced on September 20, 2023: https://www.defense.gov/News/Releases/Release/Article/3531768/deputy-secretary-of-defense-kathleen-hicks-announces-238m-chips-and-science-act/.

emerging commercial markets: electromagnetic warfare, secure-edge computing, AI hardware, quantum technology, 5G/6G technology, and commercial leap-ahead technologies. In addition to contributing to the research infrastructure, the Commons efforts support research and workforce development activities in these areas.

Photo of a research semiconductor fabrication facility. Image credit: NIST.

Section 9906(c) of the CHIPS for America Act calls for the establishment of the National Semiconductor Technology Center (NSTC).[51] In addition to conducting and supporting pre-competitive research and workforce development activities, the NSTC will establish and provide access to advanced prototyping capabilities to address the broad needs of the U.S. research community. Important features of the NSTC will include the capability to perform materials characterization, instrumentation metrology, and testing for advanced process nodes. These capabilities will enable organizations beyond just the established integrated device manufacturers to perform this type of research and increase the range of R&D that larger companies can quickly advance into manufacturing. Through close coordination with the packaging program described below in section 2.6, the NSTC will provide access to advanced test, assembly, and packaging capabilities for leading edge nodes, as well as support improvements in automation in manufacturing to provide a foundation for increasing the future U.S. share of global manufacturing capacity and competitiveness. The NSTC is envisioned as a central headquarters with affiliated technical centers that will include a combination of newly established capabilities while also

[51] https://www.nist.gov/chips/research-development-programs/national-semiconductor-technology-center

leveraging resources within existing entities.[52] Using this model, the NSTC will create and provide access to physical assets such as end-to-end prototyping facilities, digital assets, and IP, including design tools, reference flows, process design kits, and data sets, and will aggregate and manage demand for access to multi-project wafer services at commercial facilities.

While the Commons will have some efforts in the same range of technologies and device development with those supported by NSTC, the Commons has a specific set of targets in its application focus and scope of desired productization to address defense-specific priorities. Close coordination and collaboration between the NSTC and the Commons, and among the other related U.S. government efforts as discussed in Goal 4, will ensure that these efforts are synergistic and not duplicative.

Additionally, DARPA is establishing a complementary domestic R&D center for the fabrication of three-dimensional heterogeneously integrated (3DHI) microsystems under the Next-Generation Microsystems Manufacturing (NGMM) program.[53] The next major wave of microelectronics innovation is expected to come from the ability to integrate heterogeneous materials, devices, and circuits through advanced packaging, producing a tightly-coupled system that extends into the third dimension with performance that exceeds what is available from the current monolithic approach. Currently, U.S. companies engaged in 3DHI research rely on offshore facilities. This open-access domestic center for 3DHI R&D will result in a more expansive wave of innovation, will promote shared learning, and will ensure that start-ups, academia, and the defense industrial base can engage in 3DHI R&D for low-volume products. 3DHI for this center refers to the stacking of separately fabricated components from different material systems, within a single package, to produce a microsystem that provides revolutionary improvements in functionality and performance. Specifically, these microsystems will integrate disparate wafers or chips into vertically stacked architectures. Technologies involved include, but are not limited to, compound semiconductors, photonics, and MEMS systems, and extend into the power, analog, and radio frequency domains, in addition to digital logic and memory. The initial phase will focus on state-of-the-art packaging, assembly, and testing of either digital, RF, photonic, sensor, or power devices. The focus will be on developing baseline process modules, along with an initial pre-commercial 3DHI pilot-line capability and associated 3D assembly design kits. The next phase will further optimize the 3DHI process modules, add R&D efforts to increase packaging automation, and implement the operation access model for the center. The final result will be an open-access R&D center accessible by researchers in academia, small and medium-sized businesses, defense and commercial companies, and government organizations to holistically address the design, packaging, assembly, and testing of 3DHI prototypes.

Key actions to bridge the lab-to-fab gap include:

- Development of a gap analysis of current facilities followed by efforts to address capability gaps within existing facilities and establish new capabilities where needed to comprehensively address the further development of each R&D priority area identified in Goal 1.
- Establishment of agreements with international entities in allied and partner countries as necessary to provide U.S.-based researchers with access to cutting-edge manufacturing facilities to bridge current domestic gaps and facilitate collaboration.
- Development of a "fab-to-lab" ecosystem that enables researchers to bring substrates, fabricated in state-of-the-art manufacturing facilities and pre-populated with test structures

[52] *A Vision and Strategy for the National Semiconductor Technology Center*, NIST CHIPS Research and Development Office, 2023, https://www.nist.gov/system/files/documents/2023/04/27/A%20Vision%20and%20Strategy%20for%20the%20NSTC.pdf

[53] https://www.darpa.mil/news-events/2023-11-17

and/or devices, into research facilities and add novel materials or devices to enable high-throughput, high-quality measurements of innovative technologies.
- Reduction of barriers to facility access, including through outreach to the research and development community, affordable access and operating costs, and simple, equitable access models; improved access through implementation of remote access technologies and multi-project wafer programs, which can further extend the geographic reach of every facility and promote equity of access.

### 2.6: Support advanced assembly, packaging, and testing.

Innovations in the packaging, assembly, and testing of microelectronic components are key to continued U.S. leadership. As semiconductor fabrication reaches the limits of performance and efficiency improvements attainable by reducing transistor feature size, industry has turned to new approaches to enable higher performance, using 3D systems and heterogeneous integration. The current generation of high-performance devices integrate multiple technologies that include not just different silicon-based processes but also compound semiconductors, photonics, and other specialized technologies. These approaches place much greater demands on the ability to interconnect devices and subsystems—a key aspect of advanced packaging. Improvements in interconnect technology and standards for 3D and heterogeneous integration could also foster the development of a new supply chain structure for microelectronics where domestic capabilities would enhance U.S. security and competitiveness.

Advanced testing, assembly, and packaging capabilities are also needed for validation of advanced prototypes that emerge from the R&D process. Section 9906(d) of the CHIPS for America Act calls for efforts to establish an advanced packaging manufacturing program to strengthen domestic capabilities. To implement this section, the National Advanced Packaging Manufacturing Program (NAPMP)[54] has been established within NIST to support capabilities such as metrology and lithography for manufacturing, including material characterization, instrumentation, testing, and standards. The program will be aligned, closely collaborate with, and potentially leverage resources from the NSTC. As trends in leading-edge electronics are moving toward advanced heterogeneous integration, the overlap between advanced packaging and prototyping is expected to increase substantially. As is the case for other aspects of microelectronics innovation, the development and deployment of assembly, packaging, and testing capabilities need to be coordinated across the ecosystem, with direct and close communication between the manufacturing and R&D communities.

Key actions to accelerate the development of a domestic advanced packaging ecosystem include:
- Establish and closely coordinate the NGMM and NAPMP R&D and pilot manufacturing facilities to ensure that they are complementary and mutually supporting.
- Develop opportunities to enable secure sharing of ADKs, packaging-related design tools, and other digital resources in collaboration with and fully leveraging complementary efforts across the ecosystem.
- Facilitate access to chiplets, including manufacturing test vehicles, available to the packaging R&D community to enable the rapid development and testing of new chiplet integration schemes.
- Establish programs to increase the level of automation and performance of advanced packaging test and assembly equipment to enable cost-competitive domestic packaging.

[54] https://www.nist.gov/chips/research-development-programs/national-advanced-packaging-manufacturing-program

- Establish efforts focused on the development of new substrate materials and associated manufacturing technologies to support improvements in density and signal performance.
- Support industry in developing and introducing chiplet and advanced packaging standards at the right time to maximize the potential for innovation and market acceptance. NAPMP-developed manufacturing test vehicles will be used to explore and validate integration schemes and their associated standards.
- Support the development and validation of components, integration schemes, and testing methods to ensure the security of complex advanced packaged systems.

## Goal 3. Grow and Sustain the Technical Workforce for the Microelectronics R&D to Manufacturing Ecosystem

U.S. leadership in microelectronics requires a robust domestic workforce to support the entire ecosystem from research through manufacturing. An economic analysis commissioned by the semiconductor industry reported that as of 2020, both direct and indirect U.S. jobs supported by the semiconductor industry totaled 1.85 million.[55] Since the publication of that analysis in 2021, the number of people directly employed by that industry in R&D, design, and manufacturing activities in the United States increased from 277,000 to 345,000 in 2023.[56] The average pay across all educational levels for these jobs is notably higher than for other industries, consistent with Bureau of Labor Statistics data showing that workers in the semiconductor and electronic component manufacturing sector earned nearly 50% more than the average private-sector employee.[57]

High-demand STEM occupations in the industry are dominated by engineering and computer software development, and they generally require a bachelor's or advanced degree for employment. Competition for degreed professionals is increasingly at a premium, especially at the PhD level. Industry hiring for PhDs in computer and information science and in mathematics has vastly expanded during the period 2010–2019, with company hires of PhD computer and information scientists increasing by 103% and company hires of PhD mathematical scientists expanding by 160% during that period.[58] Foreign-born scientists and engineers make up 41% of the high-skilled technical workers in the semiconductor and other electronic component manufacturing sector.[59] This is consistent with data showing that foreign-born persons constitute 30% of workers in all science and engineering occupations and hold more than half the doctorates in engineering, computer science, and mathematics occupations.[60] Foreign students who complete graduate education in STEM in the United States have relatively limited options to secure permanent citizenship status, and therefore many return to their home countries or other countries with more streamlined immigration processes for highly

[55] Semiconductor Industry Association and Oxford Economics, 2021, *Chipping In, the Positive Impact of the Semiconductor Industry on the American Workforce and How Federal Industry Incentives Will Increase Domestic Jobs*, https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf

[56] Semiconductor Industry Association and Oxford Economics, 2023, *Chipping Away: Assessing and Addressing the Labor market Gap facing the U.S. Semiconductor Industry*, https://www.semiconductors.org/wp-content/uploads/2023/07/SIA_July2023_ChippingAway_website.pdf

[57] https://www.bls.gov/web/empsit/ceseeb3a.htm

[58] National Science Foundation, 2010 and 2019 National Survey of College Graduates, https://www.nsf.gov/statistics/srvygrads/

[59] Hunt and Zwentsloot, 2020, *The Chipmakers: U.S. Strengths and Priorities for the High-End Semiconductor Workforce*, https://cset.georgetown.edu/wp-content/uploads/CSET-The-Chipmakers.pdf

[60] National Center for Science and Engineering Statistics, 2020, *The State of U.S. Science and Engineering 2020*, https://ncses.nsf.gov/pubs/nsb20201/u-s-s-e-workforce

skilled immigrants.[61] In the last decade, growing fractions of the high-skilled workers educated in the United States have been returning to their home countries or other countries. Moreover, the number of domestic students choosing to enter microelectronics as a career after college has declined over the past decade.

Meeting the current and projected semiconductor talent demand will require strategies to develop, attract, and retain a larger pool of talent, both domestically and from abroad, ranging from the skilled technical workforce to doctoral-level researchers and educators. These strategies must engage the full range of stakeholders including employers, labor unions, educational institutions, government agencies, industry organizations, and programs focused on training for underrepresented and underserved populations, among others, and support the creation of positions consistent with the Good Jobs Principles.[62]

Considering the array of public and private sector reports and stakeholder input reveals several key findings and challenges related to semiconductor workforce needs. Industry competition for highly skilled talent is fierce, including international competition, compounded by an aging workforce and competition with other technology sectors. Although it is especially challenging for U.S. companies to find candidates to fill positions that require advanced degrees and U.S. citizenship, there are not enough students pursuing opportunities across all educational and job levels with the knowledge and skills needed for this workforce. Stakeholders must also work together to remove historic and entrenched systemic inequities that prevent some groups from accessing the high-paying jobs in this industry—a requirement for both increasing the domestic talent pool and maximizing innovation through a diverse and inclusive workforce.

In addition to the workforce components of the CHIPS infrastructure investments as discussed in Goal 2 above, Sec. 102(d) of the CHIPS and Science Act establishes an NSF fund for microelectronics workforce development activities. A broad scope of activities can be supported under this provision, including the development of industry-oriented curricula and teaching modules and efforts to increase the integration of microelectronics content into STEM curricula at all education levels. Learning activities and experiences can also be supported, including efforts that provide physical, simulated, and/or remote access to training facilities with industry-standard processes and tools as well as informal hands-on microelectronics learning opportunities for pre-K–12 students. In addition, this provision provides for development and implementation of research and professional development programs for teachers, and for expanding academic research capacity in microelectronics by incentivizing the hiring of faculty in fields critical to microelectronics. Ultimately, this fund paves the way for innovative education pathways that connect high school, career and technical education, military, postsecondary education, and graduate programs with industry, and enables the dissemination of materials through the creation and maintenance of a publicly-accessible database and online portal.

NSF has a long history of investing in STEM education at all levels and across settings. NSF's programs broadly invest in learners in K–12 schools, community colleges, and universities, as well as reskilling for current workers and upskilling for those seeking to enter the workforce in new and emerging areas. To prepare a diverse microelectronics and semiconductor workforce across the United States, NSF is leveraging this portfolio and building a suite of tailored investments, including scalable partnerships with the private sector to enhance the skilled semiconductor manufacturing workforce.

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[61] Congressional Research Service, 2022, *U.S. Employment-Based Immigration Policy,* https://crsreports.congress.gov/product/pdf/R/R47164

[62] https://www.dol.gov/general/good-jobs/principles

Supplementing the broad array of federal programs that support various aspects of education, research, and workforce training programs, many groups have launched or are launching efforts to address the recognized need to expand the semiconductor workforce. For example, a nonprofit organization has initiated the Growing Apprenticeships in Nanotechnology and Semiconductors (GAINS) program, funded by the Department of Labor, and with NSF support, launched the National Talent Hub, a platform for students to match with job opportunities and identify any deficiencies in their skills.[63] There are also efforts by semiconductor industry associations, including online courses developed to meet the workforce needs of their member companies.[64] Efforts and strategies to address the broader STEM workforce needs have been well documented and also apply to the semiconductor workforce.[65] The focus of this goal is on efforts where the federal government can play a role in expanding the semiconductor workforce. Connecting, scaling up, and amplifying successful programs will also be critical to meet the future workforce needs of the semiconductor industry to ensure continued U.S. leadership in microelectronics. The efforts discussed below build on these STEM education programs, with a focus on tailored efforts for the microelectronics ecosystem.

Over the next five years, efforts are needed to address the following objectives:

### 3.1: Support learners and educators in and across science and technology disciplines relevant to microelectronics.

To meet projected semiconductor workforce requirements, significant efforts will be needed to support both educators and students across the entire educational spectrum. In addition to the traditional disciplines of electrical engineering and computer science that feed into the semiconductor workforce, as the semiconductor industry continues to innovate and diversify, fields like chemistry, chemical engineering, industrial engineering, environmental engineering, and materials science and engineering will be of increasing importance. While K–12 education is the responsibility of state and local entities, much can be done to provide teachers with the resources and experience necessary for them to educate their students about the career opportunities available in microelectronics. Existing programs such as NSF's Research Experiences for Teachers (RET)[66] and the Robert Noyce Teacher Scholarship Program[67] work to recruit, train, and retain STEM teachers. For K–12 students, raising awareness of career opportunities in the semiconductor industry, along with high-quality instructional materials and exciting hands-on projects, can help inspire interest in pursuing relevant educational pathways. K–12 educators need access to high-quality teaching resources, mapped to the state standards they are required to meet.

For some skilled technical positions, non-degree programs such as certificates, certifications, diplomas, and other stackable credentials are more appropriate than traditional degree programs. The skilled technical workforce tends to have strong geographic ties, so regional efforts in current and emerging semiconductor hubs will be especially important for developing this talent. Partnerships between industry, labor, and regional training programs can help develop the knowledge and skills and define local career pathways. Industry representatives can serve as valuable mentors to students and assist educators in "train the trainer" programs. These collaborations also play an important role in facilitating regional access to industry-relevant fabrication tools and "fab-less" (digital) resources to

[63] The National Institute for Innovation and Technology, https://www.niit.org

[64] e.g., SEMI University, https://www.semi.org/en/semi-university

[65] https://www.whitehouse.gov/wp-content/uploads/2022/01/2021-CoSTEM-Progress-Report-OSTP.pdf, https://www.energy.gov/sites/default/files/2019/05/f62/STEM-Education-Strategic-Plan-2018.pdf

[66] https://www.nsf.gov/pubs/2021/nsf21606/nsf21606.htm

[67] https://www.nsf.gov/pubs/2023/nsf23586/nsf23586.htm

support education and training efforts. While there are many successful models and existing curriculum for the semiconductor technician workforce (see call-out box below), efforts to scale, share, and continually update these resources are required to have a more significant impact.

At the undergraduate and graduate levels, responsive education and training systems are needed that can adeptly adjust to the acceleration of semiconductor development and innovation.[68] The rapid pace of advancements requires engineering and science programs to remain current to avoid opening a gap between education and industry needs. In order to avoid a growing gap, industry, labor, and academia must work together in the initiation and promotion of specialized undergraduate- and graduate-level curricula and programs that are agile and able to align with emerging industry needs. Recognizing early-on that interdisciplinary approaches are necessary for the emerging challenges in semiconductor R&D will help prepare a future-focused workforce.

***Non-degree semiconductor workforce training programs***

*Non-degree programs such as the Microelectronics and Nanomanufacturing Certificate Program[69] (MNCP) from Penn State's Center for Nanotechnology Education and Utilization provide valuable training for the semiconductor workforce. The program, a partnership between community colleges and research-intensive institutions with cleanrooms, provides a semester-long classroom and experiential training that prepares student veterans to enter the microelectronics workforce. After the semester, students are ready to successfully complete three certification exams through ASTM International in Nanotechnology Characterization, Health and Safety in Nanotechnology, and Nanotechnology Fabrication and Related Infrastructure. In addition to the academic institutions, the program also has 12 U.S.-based semiconductor and microelectronics industry partners.*

Students at the UC San Diego Qualcomm Institute, an MNCP participant. Image credit: University of California.

It will be necessary to develop curricula for community college and four-year undergraduate students in emerging topics, and secure the resources to enable large cohorts of students to have immersive laboratory experiences. Relevant experiential learning is crucial for high-skilled jobs in microelectronics—coursework is not enough. However, most U.S. educational institutions do not currently have the capability and resources to provide hands-on learning experiences that fully prepare students for the microelectronics workforce. Collaborative efforts that leverage the CHIPS investments to expand the research infrastructure, as discussed above in Goal 2, will help address these needs. Utilizing virtual and augmented reality tools as well as digital twins can further help provide learning experiences at educational institutions without the physical tools. Cloud-based solutions for design, data management, modeling, and simulation could also help avoid the training gap through strengthening collaboration between industry R&D and researchers from universities and small businesses.

Activities where students work directly with industry professionals on real-world problems can be powerful learning experiences. On-the-job training models such as internship and apprenticeship programs at both public and private-sector research laboratories, development centers, and

[68] For example, see, *Getting Skills Right: Assessing and Anticipating Changing Skill Needs*, OECD, 2016, https://www.oecd.org/publications/getting-skills-right-assessing-and-anticipating-changing-skill-needs-9789264252073-en.htm.

[69] https://www.cneu.psu.edu/military-ed/

manufacturing facilities will be important to expand these opportunities. Particularly, in the most highly specialized areas, exposure to and mentorship by established industry professionals in state-of-the art facilities can help students acquire the most up-to-date skills. Public-private microelectronics training programs incorporating apprenticeships, internships, co-ops, and other on-the-job training opportunities responsive to the pace of microelectronics technology development and innovation need to be expanded across the country. Importantly, the variety of learning pathways needs to support all Americans equitably, and development should especially focus on geographic areas and populations that are currently underserved. Mechanisms, where possible, to translate apprenticeship and internship training into college credit for associate through graduate degrees will make pathways to careers in microelectronics easier to navigate.

Key actions to support learners and educators include:

- Develop a repository of high-quality instructional materials in areas relevant for semiconductor education mapped to existing standards for K–12 teachers.
- Develop a repository for curriculum, problem sets, and labs that faculty can contribute to and access to further develop their courses.
- Facilitate broad engagement in the development of these repositories to ensure that they span multiple agency programs and connect with the various CHIPS efforts to improve the sharing and leveraging of resources for educators, students, and workers.
- Promote and expand teacher training and research opportunity programs focused on semiconductors, including visiting or temporary industry exchange programs.
- Promote opportunities for teachers and students to tour major research facilities and semiconductor fabrication sites.
- Facilitate access to physical and virtual tools for teacher and student research experiences in order to provide experiential learning that will prepare students for their professional lives after completing their degrees or certifications.
- Leverage public-private and regional programs to promote mentorships, as well as on-the-job training programs such as internships and apprenticeships.
- Collaborate with professional and technical societies and industry associations to develop faculty-focused programs to better align semiconductor-related courses with industry needs.
- Facilitate sabbaticals and visiting positions for faculty in industry settings.
- Facilitate visiting scholar positions in universities for industry R&D leaders.
- Establish co-design studios to focus on interdisciplinarity and promote cross-sector exposure for students.
- Develop and deploy tools, methods, and best practices that promote inclusive and accessible use of resources and opportunities.

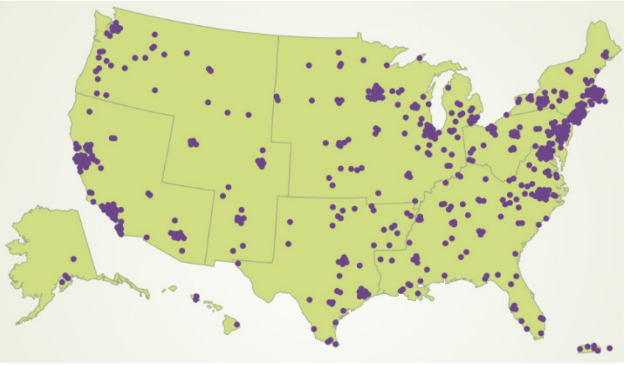
### 3.2: Foster meaningful public engagement in microelectronics and raise awareness of career opportunities in the semiconductor industry.

Informal education and engagement with the public will be critical for raising broader awareness of career opportunities in the semiconductor industry and to strengthening the domestic microelectronics workforce. As skilled semiconductor workforce needs vary by region, an emphasis on informal opportunities for communities to learn more about the industry can allow them to become active partners in the growing ecosystem. It is important to note that at the K–12 level, parents, teachers, guidance counselors, friends, and mentors, among others, influence student trajectories. Developing a shared foundational understanding of semiconductors, their applications, and workforce needs will help students make informed decisions about the opportunities that exist in the

semiconductor industry. Semiconductor-related displays and content in science centers and other places of informal STEM learning can act as easy entry points to reach people who are not currently in school, developing curiosity, interest, and broadening awareness.

***The National Informal STEM Education Network (NISE Network)***

*NISE Network[70] is a robust community of science education experts across the country, primarily consisting of local museums and university outreach educators who collaborate with local libraries, community centers, and schools. NISE Network originated as the Nanoscale Informal Science Education Network, which was supported by NSF from 2005–2016. The original NISE Net reached over 30 million people with a focus on fostering an awareness and understanding of nanotechnology. NISE Net continues to add to the catalog of educational materials for many subjects relevant to the microelectronics workforce. The more than 600 NISE Network partners can be found in all U.S. states and territories, providing access to these lessons across all of America.*



Map showing NISE Network participating institutions. Image credit: National Informal STEM Education Network, Report to Partners 2005-2016.

Strategies to raise awareness of opportunities in the semiconductor industry include:

- Leverage programs that develop museum exhibits and publicly available activities that are connected to vetted, actionable information and that broaden understanding of semiconductors and their applications.
- Build or connect to existing networks of informal science centers, so regional experts with an understanding of local needs and concerns can contribute to content development.
- Develop and distribute teaching and demonstration kits that can be leveraged during an annual event or celebration around microelectronics.[71]
- Fully utilize multimedia and social media tools to broaden reach and awareness across all of America.
- Utilize competitions and challenges to raise awareness and motivate students to compete around semiconductor issues.

### 3.3: Prepare an inclusive current and future microelectronics workforce.

Expanding microelectronics and related education across the country, including efforts targeted at smaller and rural schools, community colleges, Historically Black Colleges and Universities (HBCUs), Tribally Controlled Colleges and Universities (TCCUs), and other minority-serving institutions (MSIs), will provide opportunities to talent currently underrepresented in the semiconductor industry. Increasingly diverse representation within the semiconductor workforce will support innovation and foster a more inclusive and positive professional environment, which in turn will attract more talent. Bridging programs can help address opportunity gaps to ensure that efforts reach all of America. As students move from high school to degree programs and from undergraduate to graduate school, bridging programs can strengthen the foundational skills and knowledge necessary to succeed. Efforts

[70] https://nisenet.org

[71] For example, similar to the NanoDays kits distributed by the NSF-funded NISE Network https://www.nisenet.org/nanodays

to provide wrap-around services, such as childcare, may help attract dual-career researchers and have a multiplicative impact.

Addressing current and future microelectronics workforce challenges will require the development and use of skill-need inventories among educators, trainers, policymakers, labor unions, professional societies, and industry. Identification of common knowledge, skills, and abilities (KSAs) and technical competencies within the microelectronics industry must be done through the collaboration of relevant parties. Mapping of KSAs to curriculum, technical and vocational education, and career guidance for learners will increase student readiness to join the semiconductor workforce. This effort needs to be regularly updated to keep pace with industry innovation.

Internships are many students' first experiences with the exciting and promising applications of the STEM knowledge they have been developing in the classroom. Ensuring that these opportunities are available at the key transition from the first to second year of higher education can provide early exposure to career possibilities and strengthen student connection to the semiconductor industry. The federal government already has significant investments in microelectronics internship programs across agencies. For example, NIST offers paid summer internships to students in high school, four-year universities, community colleges, vocational schools, and other various educational programs.[72] NSF recently established a partnership with the Semiconductor Research Corporation to develop new sites of the NSF Research Experiences for Undergraduates (REU) program related to advancements in semiconductors.[73] This new partnership will ensure that there are multiple cohorts dedicated to microelectronics research, helping these students prepare for graduate research and/or careers in the field. The NSF Experiential Learning for Emerging and Novel Technologies (ExLENT) program is designed to provide inclusive experiential learning experiences to develop the workforce for emerging technologies, including semiconductors and microelectronics.[74] In addition, DOE supports internships for thousands of students at its 17 National Laboratories, allowing students to obtain experiential learning in high school, technical schools, colleges and universities, and other educational programs. DOE also supports graduate and post-doctoral fellowships at its national laboratories and at many universities and colleges.

Mechanisms are also needed to more easily recruit and retain foreign students and professionals to meet the workforce demands of the U.S. microelectronics industry. Building and retaining the domestic workforce at advanced degree levels will also require incentives to compete with recruitment efforts by other nations, including improved immigration pathways for foreign-born, U.S.-educated students with key R&D and manufacturing-related skills.[75] Appropriately vetted international student exchanges to further broaden access to fabrication facilities and secure cooperation with international allies and partners can also encourage skilled foreign students to support U.S. workforce needs. Programs to expand education pathways from other countries, especially countries underrepresented in U.S. higher education, would support workforce demands and accelerate the needed growth. Examples in this space include programs that expose students from other countries to academic research explorations,

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72 https://www.nist.gov/careers/student-opportunities/internship-program

73 https://www.nsf.gov/pubs/2023/nsf23601/nsf23601.htm

74 https://www.nsf.gov/pubs/2023/nsf23507/nsf23507.htm

75 National Science Board, 2022, *International STEM Talent is Crucial for a Robust U.S. Economy*, https://www.nsf.gov/nsb/sei/one-pagers/NSB-International-STEM-Talent-2022.pdf; U.S. Government Accountability Office, 2022, *Semiconductor Supply Chain: Policy Considerations from Selected Experts for Reducing Risks and Mitigating Shortages*, https://www.gao.gov/assets/gao-22-105923.pdf; Congressional Research Service, 2022, *U.S. Employment-Based Immigration Policy,* https://crsreports.congress.gov/product/pdf/R/R47164; Krol, 2021, *Effects of Immigration on Entrepreneurship and Innovation*, https://www.cato.org/sites/cato.org/files/2021-10/cj-41n3-5.pdf

thus promoting enrollment in master's and doctoral programs. Research protection remains paramount, but such concerns must be balanced with the positive role international talent has played, and will continue to play, in the U.S. innovation ecosystem.[76]

Students learning to use sophisticated equipment at one of the NNCI user sites. Image credit: Cornell University.

Strategies to help prepare the microelectronics workforce include:

- Intentionally engage with and share educational programs and opportunities across the United States, ensuring geographic diversity as well as connections to HBCUs, TCCUs, MSIs, and four-year and community colleges.
- Improve the accessibility of microelectronics educational programming to enable access for students with disabilities and diverse learning styles.
- Encourage industry, academia, and other relevant stakeholders to work together to identify, update, and map KSAs and technical competencies to jobs across the semiconductor supply chain.
- Expand existing paid internships and fellowships for students training in microelectronics.
- Develop an open platform with low- or no-cost online courses and stackable credentials for future workforce development that provides career-spanning opportunities for re/upskilling.
- Offer remote, virtual, and/or augmented reality training to simulate the fabrication environment.
- Develop mechanisms to recruit and retain appropriately vetted foreign students and researchers.

### 3.4: Build and drive microelectronics research and innovation capacity.

In order for the United States to increase its competitiveness, it must prioritize investments and strategic programs that support innovation and entrepreneurship. There are opportunities to increase product quality, decrease costs, and maximize efficiencies to support semiconductor facilities. There is a need to incentivize students at later stages in their education to embark on research careers. This is especially important for first-generation college students in underserved communities who may not have the role models, mentors, or resources to decide their career paths at such an early age. The NSF-supported Non-Academic Research Internships for Graduate Students (INTERN) program provides graduate students with the financial support to work outside the academic setting so they can develop the professional skills industry needs.[77] Additionally, students at all stages often change their interests or career plans, and agile and flexible systems will be required for redirecting students—and the existing workforce—into new careers such as research and development.

In addition to the people necessary to meet present and future workforce needs, the learning process requires access to state-of-the-art facilities, equipment, and tools. As discussed above in Goal 2, increased resource-sharing, co-location, virtual learning environments, and other means are needed to

[76] Science and Technology Policy Institute, 2021, *Economic Benefits and Losses from Foreign STEM Talent in the United States*, https://www.ida.org/research-and-publications/publications/all/e/ec/economic-benefits-and-losses-from-foreign-stem-talent-in-the-united-states; National Science and Technology Council, Subcommittee on Economic and Security Implications of Quantum Science, 2021, *The Role of International Talent in Quantum Information Science*, https://www.quantum.gov/wp-content/uploads/2021/10/2021_NSTC_ESIX_INTL_TALENT_QIS.pdf

[77] https://www.nsf.gov/eng/eec/intern.jsp

provide students associated with a specific academic institution with access to vital learning resources across multiple institutions or facilities. As infrastructure expands to support R&D, students also require access to these resources. Barriers to access can be minimized through remote access technologies, travel funding to remove geographic constraints on students' ability to work with leading-edge tools, and mechanisms that make it easy for students to cross academic systems as they pursue their innovative work.

***Attracting and retaining students early in their academic careers***

*In order to expand the microelectronics research ecosystem, programs need to attract and retain students early in their academic careers and encourage them to pursue advanced degree programs. The DOD-supported Scalable Asymmetric Lifecycle Engagement (SCALE) program combines DOD governance with input from a national public-private academic partnership to attract, develop, and retain a clearable microelectronics workforce. SCALE is an immersive educational program that combines government and defense industrial base internships with aligned research and mentoring to deepen understanding and relationship-building for U.S. citizen undergraduate and graduate students. To achieve these goals, SCALE has developed a set of national curriculum standards; a cohesive messaging and recruiting approach tailored to students ranging from K–12 through PhD; an industry-supported Center for Secure Microelectronics Ecosystem to engage students in transitioning research to specific missions; and systematic programmatic evaluation to ensure increased effectiveness in training and retaining students to meet workforce needs.*

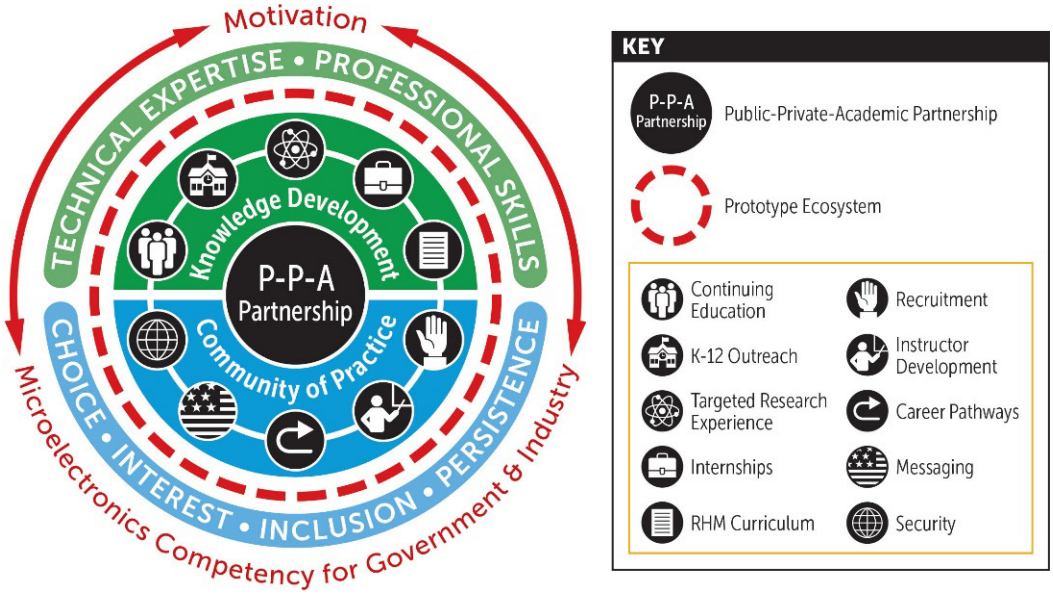


Image credit: Purdue University.[78]

Strategies to help grow and sustain the research and development workforce include:

- Leverage college and university entrepreneurship programs, including an emphasis in business schools, to expand interest in building the economic conditions for advancing U.S. leadership.
- Increase fellowships for students to pursue advanced degrees in STEM-related disciplines focused on research, innovation, and entrepreneurship.

[78] Moore, T.J., Douglas, K.A., & Bermel, P. (2020). *SCALE framework for workforce development for defense microelectronics*. Presented at the SCALE Trusted and Assured Microelectronics Kickoff meeting, Indianapolis, IN.

- Provide mechanisms such as travel grants for students to more easily access the research infrastructure, as discussed in goal 2, enabling them to train and work across the research development pathway.
- Offer scholarships; undergraduate, graduate, and postdoctoral fellowships; and other work-based learning opportunities for applied-research experiences.
- Explore opportunities to facilitate more exchange programs or externships between academic institutions and industry.

## Goal 4. Create a Vibrant Microelectronics Innovation Ecosystem to Accelerate the Transition of R&D to U.S. Industry

The historic investments enabled by the CHIPS Acts provide not only an opportunity to fill existing gaps in the R&D infrastructure, but also to revitalize the ecosystem and create a virtuous microelectronics innovation cycle. The current division of disciplines, institutions, academia, and industry, coupled with challenges traversing facilities and negotiating complex agreements to access tools and digital resources, presents serious obstacles as new innovations mature along the technology development continuum. The strategies discussed below aim to reduce or eliminate these obstacles to promote collaboration across the stack, facilitate access to research infrastructure, promote academia-industry-government collaboration, and build bridges between various efforts to create a network of pathways, feedback loops, and hand-offs to enable new innovations to accelerate transition into the market.

***An interconnected, complex, research ecosystem***

*As noted throughout this report, the microelectronics R&D ecosystem is complex and infrastructure-intensive. Networks of user facilities have expanded access to the specialized tools required to fabricate and characterize new materials and devices. These user facilities have been described as "democratizing science" by enabling researchers at institutions without the resources to build out full toolsets to contribute to microelectronics research, and expands the innovation base for new advances. The NSF-funded National Nanotechnology Coordinated Infrastructure is one of the user networks that provides access to thousands of specialized tools critical for microelectronics research. In this network diagram (left), the NNCI sites are depicted in black, and the grey dots represent academic institutions that have used NNCI facilities. As illustrated in the diagram, each facility is used by many universities, and many universities make use of multiple sites, reflecting the complexity of the ecosystem and the far-reaching impact these user facilities have on the research enterprise, helping to connect different innovators and programs.*

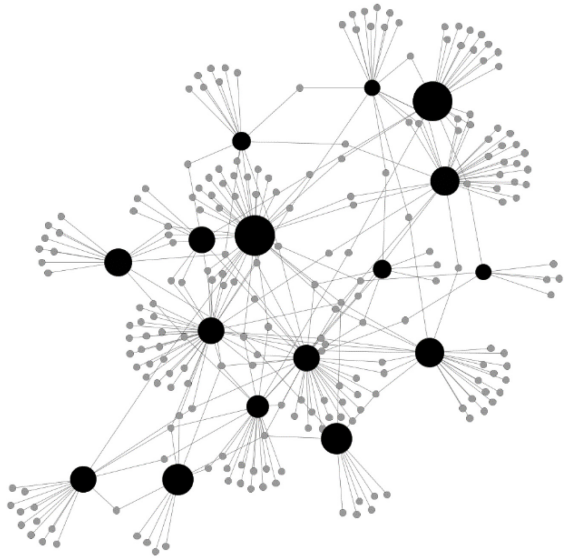

Diagram of the NNCI network. Image credit: OSTP.

A vibrant ecosystem includes all aspects of technology development from an early research concept through incorporation into a system or product. Entities that are part of the ecosystem include academic institutions, small and large companies across the supply chain, nonprofit consortia and associations, National Laboratories and other FFRDCs, start-ups, investment firms, and departments and agencies from federal, state, regional, and local government. In addition to research and

technology development, the ecosystem must include the education and training efforts required to ensure that the appropriate workforce is available for every stage of the process. Participants include students and educators, researchers, developers, scientists and engineers, entrepreneurs, union officials, business leaders, and policymakers.

The long time horizons needed to transition R&D into commercial practice present additional challenges. New technologies often take 10−15 years from the time research is published to when the innovation reaches volume commercial manufacturing. Technologies that rely on complex scientific breakthroughs can take substantially longer. For example, extreme ultraviolet lithography tools took more than 40 years to be incorporated into high-volume manufacturing. Federal support and enhanced coordination across stakeholders, as outlined below, can help address this challenge and accelerate the research, development, demonstration, and deployment cycle.

There is strong agreement among public and private-sector stakeholders that maintaining leadership in the semiconductor industry will require the United States to innovate *at a faster pace* than competitors.[79] Accelerating the rate at which R&D is translated into products and services is essential to deriving broad benefits for the public, supporting the U.S. economy, and sustaining national security. A vibrant culture of innovation, focused on areas identified in Goal 1, is a critical foundation that must be complemented by resources and policies to accelerate the translation of those innovations. Sustained leadership requires the creation and support of a virtuous cycle, where R&D drives innovative market-ready technology development incorporating both incremental and transformational advancements, and in turn those technologies drive new insights and funding for R&D. This combination of excellence in R&D coupled with *rapidly* transitioning R&D into products and services will be an essential and distinctive competitive advantage for the United States and its allies.

Mechanisms are required to increase communication and collaboration between and among agencies, and across academic, government, and industrial R&D communities. Such communication and collaboration are essential for connecting R&D performers with end users in government and industry and enhancing researchers' knowledge of system-level design and performance constraints. Enhanced communication and collaboration can inform research directions to ensure that advancements can be implemented and increase the likelihood that innovative concepts are transitioned to manufacturing. Furthermore, building communication pathways and collaboration will provide opportunities for new research advances to fuel disruptive innovations that can leapfrog existing technologies.

To develop the vibrant microelectronics ecosystem that will accelerate transition of R&D to commercialization, U.S. government efforts over the next five years will address the following objectives:

### 4.1: Support, build, and bridge centers, public private partnerships, and consortia to deepen collaboration among various stakeholders in the microelectronics ecosystem.

Federal agencies regularly collaborate together, and directly with companies from across the microelectronics sector, on research areas of mutual interest, and industry often engages directly with

[79] For example, see *Report on Ensuring Long-Term U.S. Leadership in Semiconductors,* Presidents Council of Advisors on Science and Technology, 2017, https://obamawhitehouse.archives.gov/sites/default/files/microsites/ostp/PCAST/pcast_ensuring_long-term_us_leadership_in_semiconductors.pdf; *Winning the Future. A Blueprint for Sustained U.S. Leadership in Semiconductor Technology*, Semiconductor Industry Association, 2019, https://www.semiconductors.org/wp-content/uploads/2019/04/SIA_Winning-the-Future_Refresh_FINAL1.pdf; and *Final Report*, National Security Commission on Artificial Intelligence, 2021, https://www.nscai.gov/wp-content/uploads/2021/03/Full-Report-Digital-1.pdf.

individual academic research groups for specific programs. Ensuring microelectronics leadership into the future, however, requires deepening collaboration to address critical present and future challenges. Major research centers and public-private partnerships, where appropriate, can bring multiple parties together. The establishment and sustained support of these efforts has proven to be an effective approach to facilitate collaboration focused on specific technical challenges addressed by strategically assembled teams. For example, some federal agencies have partnered with the Semiconductor Research Corporation (SRC) as an approach to couple fundamental academic research more tightly to longer-term industry technology and workforce needs. The success of this approach is epitomized by the DARPA-SRC Joint University Microelectronics Program (JUMP 2.0)[80] and its predecessors. While industry often has bilateral agreements with specific academic investigators, federally funded programs such as JUMP facilitate broader cross-industry information exchange and consensus building. With a broader community perspective, these collaboration structures more quickly identify the highest priority research to fund. These structures also provide rapid feedback from the industry partners to the academic researchers, with government participants helping to ensure a broad impact and public-sector return on investment. The focused efforts discussed in this section to deepen collaboration will enable:

- Early identification of a more comprehensive set of potential roadblocks to the maturation and scaling of new technologies for investigation by a wider set of industry and scientific experts and the design of both public and private funding programs to support that work.
- A broader recognition of both shared and unique needs across different segments of the ecosystem, including the needs of educational programs, academic researchers, government-funded and independent research laboratories, and small businesses, and the development of new products, product fee structures, and services to address those needs.
- The establishment of new methodologies for the development and maturation of new technologies and techniques that creatively leverage the distinctive capabilities of many different partnering organizations, including the world-leading instrumentation and other resources at government-funded user facilities and highly specialized enterprises.
- The concentration of resources from both public and private sources on advancing potentially transformative technologies through development phases where costs grow significantly while fundamental risks to eventual technical success and commercial viability remain high, thus enabling more innovations to reach market relevance more quickly than current practice.

In addition to the user facilities discussed above, NSF has several programs that support large multi-institutional research centers that include industry and other members. The centers bring together academic researchers to collaborate on common challenges and leverage capabilities. These programs also provide a framework for membership agreements with small and large companies and other entities that address key issues such as intellectual property considerations. There are currently several NSF centers that are relevant to microelectronics R&D, including the NSF Engineering Research Center, Nanomanufacturing Systems for Mobile Computing and Energy Technologies (NASCENT),[81] focused on the creation of revolutionary manufacturing, devices, materials, and modeling that includes small and large companies representing research institutions, materials suppliers, equipment manufacturers, integrated device manufacturers, and a leading-edge foundry. Other examples include several centers funded under the NSF Industry-University Cooperative Research Centers (IUCRC) program[82] (in which NSF provides operating funds and industry provides the majority of research funding), e.g., the Center

[80] https://www.src.org/program/jump2/ and https://www.darpa.mil/news-events/2023-01-04

[81] https://www.nsf.gov/awardsearch/showAward?AWD_ID=1160494

[82] https://iucrc.nsf.gov/

for Hardware and Embedded Systems Security and Trust (CHEST)[83] and the Center for High Frequency Electronics & Circuits for Communication Systems (CHECCS).[84]

Innovation in microelectronics and semiconductor technologies at DOE's 17 National Laboratories is enabled by a preeminent base of expertise in physics; chemistry and chemical engineering; materials science; plasma science; isotope production; nanofabrication; electrical, mechanical, and systems engineering; and computer science. Complementing this expertise is a broad range of capabilities for materials research, device design and fabrication, characterization, and modeling and simulation. Specific capabilities required for the development of advanced microelectronics exist across DOE's National Laboratories, including development and assessment of new materials and rapid prototyping via novel fabrication approaches available through the DOE's five Nanoscale Science Research Centers and other user facilities. Additional R&D and production capabilities are available at facilities such as the Microsystems Engineering, Science and Applications (MESA) complex at Sandia National Laboratories. Complementing these experimental capabilities are simulation, modeling, and data science capabilities ranging from atomistic methods to quantum and neuromorphic techniques, artificial intelligence and machine learning, and beyond-exascale high-performance computing (HPC). HPC provides capabilities to support materials research, circuit and system design, and performance prediction. Many of these experimental and computational capabilities are available to the broad scientific community, including universities, industry, and other government agencies through DOE's network of user facilities.[85]

Regional innovation hubs can bring together multiple partners and facilitate technology transfer along the lab-to-market pathway by coordination across the supply chain. Partnership-based regional hubs have the potential to reduce the time and cost for development and transition by combining the management capacity of large businesses with the niche expertise residing in smaller businesses, government, and academic research laboratories. Regional hubs have been shown to be most effective when enhancing existing clusters rather than attempting to create such ecosystems without an existing base of capital and talent.[86] The NSF Regional Innovation Engines[87] and DOC Economic Development Administration Regional Technology and Innovation Hubs (Tech Hubs)[88] programs are examples of federal programs to support these efforts. Additionally, the DOC CHIPS Incentives Program encourages efforts to support regional semiconductor ecosystems.[89]

The DOD Microelectronics Commons has been designed to leverage and strengthen regional ecosystems around selected hubs that provide lab-to-fab capabilities. The Commons hub ecosystems, not necessarily limited by state boundaries, are intended to be networks of regional capabilities that leverage, with potential augmentation using Commons' funding, existing capabilities at academic, nonprofit, or industry facilities, which can serve as sources of innovation as well as hosts for sponsored efforts.

The Manufacturing USA institutes represent another effective model for fostering exchange between industry needs and academic capabilities across multiple manufacturing-based industries. Presently,

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83 https://iucrc.nsf.gov/centers/center-for-hardware-and-embedded-system-security-and-trust/

84 https://iucrc.nsf.gov/centers/center-for-high-frequency-electronics-and-circuits-for-communication-systems-checcs/

85 DOE Office of Science User Facilities, https://science.osti.gov/User-Facilities/User-Facilities-at-a-Glance; all DOE user facilities, https://www.energy.gov/gc/articles/doe-designated-user-facilities

86 Rethinking Cluster Initiatives, 2018, https://www.brookings.edu/wp-content/uploads/2018/07/201807_Brookings-Metro_Rethinking-Clusters-Initiatives_Full-report-final.pdf

87 https://new.nsf.gov/funding/initiatives/regional-innovation-engines

88 https://www.eda.gov/funding/programs/regional-technology-and-innovation-hubs

89 https://applications.chips.gov/s/

five institutes support elements of the microelectronics manufacturing base, including the adjacent sectors of additive manufacturing and 3D printing, advanced robotics for manufacturing, and digital tools for manufacturing. Additional engagement with these and other sectors that rely on microelectronics innovation, such as industrial automation and robotics, communications, high-performance and next-generation computing, health sciences, and artificial intelligence, would help inform new areas for collaboration. Under the CHIPS Acts, Congress authorized and appropriated resources for the establishment of up to three new Manufacturing USA institutes focused on semiconductor manufacturing. Increased support for new and existing models can extend to new and emerging technologies and engage new industry partners, both large and small, to accelerate the transition of new technologies to manufacturing.

The National Semiconductor Technology Center is envisioned to be the focal point for the U.S. microelectronics innovation ecosystem.[90] As detailed in Section 9906(c) of the CHIPS for America Act, the NSTC will be a public-private consortium that includes DOC, DOD, DOE, and NSF, as well as private-sector entities. While many of the details of the NSTC are still in development, it will seek to bring in members from across the entire microelectronics value chain—including small and large companies, universities, research organizations, DOE National Laboratories and other FFRDCs, and nonprofits—and will establish mechanisms to facilitate information exchange, entice private-sector investment from both members and outside investors, and coordinate private and public-sector investment. Enabling these roles requires the NSTC to both be trusted as a neutral coordinator and viewed as responsive to the needs of both its public and private funders, and this requires both world-leading technical expertise and a governance structure that will appropriately balance public and private-sector interests.

In addition to providing access to physical assets through a network of technical centers discussed under Goal 2, the NSTC will likely engage in several of the strategies highlighted here to help connect the community. In additional to key tools, the constellation of microelectronics R&D facilities must also have a critical mass of technical experts and scientific researchers to operate and advance the instrumentation, and to create a center of excellence to address key issues outside the purview of other entities. For example, academic researchers may discover a new material and conduct experiments and prototyping to prove out the concept. In order for a new material to be adopted into design and use, however, the defect structure must be exquisitely understood under various processing parameters to fully predict its behavior and performance. This targeted research is beyond the role of an academic effort, but unlikely to be addressed in an industrial laboratory because the material hasn't been fully proven. The same concept is true across the stack; necessary research falls between early-stage research and later-stage implementation, forming a gap in the current U.S. ecosystem. The efforts identified in this report are designed to fill this gap, providing access to both the required infrastructure and the scientific expertise needed to help transition innovations across the technology development pathway by leveraging public and private investments and expertise from across the ecosystem. For example, the NSTC will complement dedicated professional scientific staff with visiting scientists, rotators, detailees, and others from academia, industry, DOE National Laboratories and other FFRDCs, and other facilities from around the world to create a vibrant innovation engine to accelerate the adoption of future innovations into manufacturing.[91]

[90] *A Vision and Strategy for the National Semiconductor Technology Center*, NIST CHIPS Research and Development Office, 2023, https://www.nist.gov/system/files/documents/2023/04/27/A%20Vision%20and%20Strategy%20for%20the%20NSTC.pdf

[91] ibid

While each of these approaches facilitates knowledge and talent flow within each specific effort, communication across the full microelectronics technology development continuum must be facilitated to support and strengthen the entire ecosystem. In some cases, direct connections between consortia with membership or other contractual agreements may be required, while in other cases, less formal arrangements may be sufficient or preferred. The pathways to mature and transition research breakthroughs, traversing the constellation of infrastructure resources as well the scientific expertise, need to be identified and supported. The technology development pathway isn't a simple linear process, so feedback loops and branches will be necessary. It is also important to note that a single researcher or research team rarely carries a new innovation along its entire development journey, so hand-offs between entities also need to be facilitated.

Key actions to facilitate information sharing and collaboration between and among the many centers and consortia include:

- Deepen collaboration among government officials from the many agencies that oversee, support, and provide guidance to relevant centers and consortia through the SML structure, advisory boards, and other mechanisms as appropriate.
- Designate a representative from each agency to serve as a guide to help stakeholders navigate the complex network of facilities and funding opportunities as researchers move through the stages of technology development. These guides will work closely together through the SML and collaborate with center/consortia leadership.
- Develop and publish detailed information regarding capabilities and specific tools available within each center/consortium.
- Convene center directors, along with agency sponsors, on an annual basis to build community and raise awareness of capabilities and activities across the ecosystem.
- Support shared events and webinars to increase awareness among researchers of other centers' efforts.
- Promote research exchanges and visiting positions across centers.
- Include representatives from each of the primary U.S. government agencies supporting microelectronics R&D on review committees and performers' events to leverage federal funds.
- Develop access agreements between consortia, where appropriate.
- Leverage training efforts[92] on issues including patents and other intellectual property, and standards development to raise researchers' awareness of key steps to commercialization.
- Conduct an annual SML review of capabilities, along with regular RFIs to solicit input from stakeholders.

### 4.2: Engage with and leverage the CHIPS Industrial Advisory Committee.

Strengthening and revitalizing U.S. leadership in microelectronics will require close engagement, advice, and oversight from a broad cohort of industry and academic stakeholders. As called for in Section 9906(b) of the CHIPS for America Act of 2021, the Secretary of Commerce has established an Industrial Advisory Committee (IAC) to assess and provide guidance to the U.S. government on the science and technology needs of the nation's domestic microelectronics industry; analyze the extent to which this National Strategy on Microelectronics Research is helping maintain U.S. leadership in microelectronics manufacturing; assess the research and development programs and activities authorized under the CHIPS for America Act of 2021; and identify opportunities for new public-private

[92] For example, I-Corps (https://new.nsf.gov/funding/initiatives/i-corps) and programs at the U.S. Patent and Trademark Office (https://www.uspto.gov/patents/training) and the Small Business Administration (https://www.sba.gov/about-sba/sba-locations/headquarters-offices/office-entrepreneurship-education)

partnerships to advance microelectronics research, development, and domestic manufacturing. This federal advisory committee, which provides regular reports to the Secretary of Commerce, will also be valuable in proactively identifying emerging R&D, manufacturing technology, and workforce needs in response to future strategic shifts in commercial markets or geopolitics.

The IAC has initiated its work with the establishment of its working groups on Organizational and Public-Private Partnerships, R&D Workforce, and R&D. More information regarding the tasking of and recommendations from each of these working groups is available on the IAC website.[93]

At its first meeting, the Committee was briefed on a draft of this National Strategy on Microelectronics Research and public responses received from the Request for Information posted in the Federal Register.[94] The discussion and subsequent recommendations released by the IAC informed revisions to this document.

Key actions to engage and leverage the CHIPS IAC include:

- Review of IAC recommendations by the SML to inform interagency discussion and agency actions.
- Briefing updates to the IAC by agency representatives, as requested and appropriate.

### 4.3: Motivate and align the microelectronics community on key technical challenges with R&D roadmaps and grand challenges.

There is a long history of the effective use of roadmaps in the semiconductor industry to align research efforts and corresponding investments with the key technical challenges as technology advanced to ever smaller nodes. Industry technology roadmaps can be incredibly valuable, if they are widely trusted and frequently refreshed, in enabling innovation by focusing innovators and providing investors with confidence in timelines for commercial viability. Moreover, such roadmaps define the frontiers of what expected progress is anticipated to provide, which motivates innovative R&D that might exceed those expectations. The diversification of microelectronics, as discussed in Goal 1, will require multiple roadmaps to support the various performance metrics for different applications. The federal government will continue to encourage, and fund where appropriate, the development of technology roadmaps developed by community stakeholders and informed by the latest understanding of relevant technical and economic factors.

Another mechanism for motivating and organizing the R&D community is the articulation of grand challenges to help identify priority R&D directions. These activities must broadly represent and engage stakeholders from academic institutions, research laboratories, and industry. They must also focus on topics that need a wide diversity of expertise to realize non-incremental progress and advance the industry as a whole.

Key strategies to promote the development of roadmaps and grand challenges to focus research efforts include:

- Convening workshops and meetings to bring the community together to identify and address key issues.
- Supporting efforts of industry associations and other organizations leading roadmapping efforts.

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93 https://www.nist.gov/chips/industrial-advisory-committee

94 *Draft National Strategy on Microelectronics Research*, OSTP, 2022, https://www.federalregister.gov/documents/2022/09/15/2022-19935/request-for-information-draft-national-strategy-on-microelectronics-research

### 4.4: Facilitate academic, government, and industrial exchange to broaden understanding of needs and opportunities.

In addition to student internships, opportunities for faculty to spend time in industrial R&D or manufacturing settings, or in federal research facilities, can provide valuable experience and insight. Likewise, embedding industry researchers in academic centers can promote information exchange and provide context to the university research community.

As technology continues to advance, and developments increasingly rely on ever-more-precisely-engineered materials and processes, the instrumentation, diagnostics, and experimental synthesis capabilities needed to quickly mature new ideas will fall increasingly out of reach of even large private enterprises. As a result, the roles played by world-leading instrumentation, synthesis capabilities, and computing resources at government-funded user facilities and other research institutions, notably at DOE National Laboratories and other FFRDCs, are anticipated to become increasingly critical to the innovation pipeline. Enabling that role requires:

- Developing efficient partnering methods between government-funded institutions and private-sector organizations enabling fair and flexible short- and long-term arrangements that minimize the time consumed by contractual negotiations.
- Including an expanded set of potential stakeholders when agencies are gathering requirements and conducting technical and programmatic planning for government-funded resources and activities, including understanding how private funding might be used to expand publicly-funded programs while ensuring that those programs meet mission needs.
- Expanding activities that spread awareness of available government-funded capabilities and enabling use of those capabilities by programs aimed at education and workforce development in addition to programs aimed at growing public-private partnerships.

### 4.5: Support entrepreneurship, start-ups, and early-stage businesses through targeted programs and investments.

The history of Silicon Valley is a testimony to the enormous role played by start-ups in driving innovation within the microelectronics sector. However, trends such as the high capital costs to design and fabricate leading-edge circuits and the consolidation of the manufacturing sector have created a particularly large mismatch between the needs of start-ups and how innovation occurs in large multinational corporations. In view of these challenges, targeted federal investments are needed to catalyze the creation and promote the success of early-stage companies striving to bring new technologies to market.

Federally funded programs can provide entrepreneurs with business-development training and access to R&D infrastructure, and can help initiate private-sector partnerships and capital investments. Multiple federal programs have been established to support entrepreneurship that could be scaled and/or replicated to provide opportunities specific to this sector, including the following examples:

- The Innovation Corps (I-Corps) program[95] at NSF provides training to academics to facilitate the formation of start-ups by advancing their understanding of business planning and entrepreneurial skills. DOE's Energy I-Corps does the same for entrepreneurs based at DOE National Laboratories.

[95] https://new.nsf.gov/funding/initiatives/i-corps

- The NSF Convergence Accelerator program[96] provides researchers and innovators with the knowledge and opportunity to accelerate solutions into real-world applications by supporting interdisciplinary teams comprised of diverse expertise, disciplines, sectors, and communities of practice working together to stimulate innovation and discovery.
- DOE's Advanced Materials and Manufacturing Technologies Office has established embedded entrepreneur programs at four DOE National Laboratories to help innovative start-ups develop new manufacturing technologies and bring them to market more quickly through access to the labs' expertise and scientific infrastructure.[97]
- The NIST Technology Maturation Accelerator Program[98] provides a platform for NIST researchers to pitch cutting-edge technologies to venture capitalists and business experts, with the winners to receive funding to accelerate their projects toward the market.
- NASA has launched an Entrepreneurs Challenge[99] to identify innovative ideas and new participants that will lead to new instruments and technologies with the potential to advance the agency's science mission goals.
- DARPA created the Embedded Entrepreneurship Initiative[100] to accelerate the commercialization of sponsored research. The initiative funds development of a market strategy, and teams with the Intelligence Community's In-Q-Tel (IQT) venture arm to provide mentorship and investor connections.[101] DARPA has also leveraged the Cyclotron Road site from DOE's Lab-embedded Entrepreneurship Program to sponsor fellowships specifically for microelectronics start-ups.

Agency Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs offer another opportunity to support small businesses, both through non-dilutive capital investments and through a wide range of support services to promote the success of the supported companies. There are examples where agencies have coordinated their SBIR/STTR solicitations to support specific technologies of common interest. Coordinating SBIR/STTR topics across agencies can signal commitment and interest in U.S. innovation and emerging technologies, especially for start-ups and small businesses in fields related to the semiconductor industry. As an example, the SBIR/STTR program at the Department of Agriculture's National Institute of Food and Agriculture has funded a project that applies microelectronics technologies to agriculture, including a micro-sensor suite that provides growers with a direct physical measurement of plant water stress for the purpose of irrigation scheduling. Joint agency topics can be used to establish a wide community of practice that intentionally incorporates innovative small businesses and expands connections with accelerators at universities, including at HBCUs and other MSIs.

The U.S. Air Force's commercial "investment" group, AFVentures, is an example of an approach for leveraging an SBIR/STTR program to accelerate technology transition by providing additional funds to match private investments in companies in the portfolio.[102] This program increased the percentage of companies with awards that have received some form of venture capital to 29%, compared to only 10%

96 https://new.nsf.gov/funding/initiatives/convergence-accelerator

97 DOE AMMTO's Laboratory Embedded Entrepreneurship Program (LEEP), https://www.energy.gov/eere/ammto/lab-embedded-entrepreneurship-program

98 https://www.nist.gov/news-events/news/2021/06/recap-tmap

99 https://www.nasa.gov/nasa-entrepreneurs-challenge

100 https://eei.darpa.mil/

101 https://www.iqt.org/news/iqt-emerge-teams-with-darpa-to-promote-technology-commercialization-to-benefit-u-s-national-security/

102 https://afwerx.com/afventures-overview/

across all DOD awardees prior to 2015.[103] The AFVentures portfolio presently includes electronics companies as only a small portion of the total awards.

There are a few federal government programs that use venture funds for equity financing to directly support early-stage companies and partner with the private-sector venture community. For example, IQT supports technologies for the intelligence community,[104] and HHS's Biomedical Advanced Research and Development Authority (BARDA) recently launched BARDA Ventures[105] to support medical countermeasures for public health. Coupling venture capital funds to research infrastructure through public-private partnerships that incorporate technology transfer objectives has shown proven returns in the microelectronics sector in other countries.[106] The venture funds can provide a more direct pathway to support commercialization of the innovations created at the collaborative facility. CHIPS for America Act provisions call for an investment fund within the NSTC. Details for this fund are under development.

Loans and loan guarantees are another mechanism that can assist early-stage companies. The Small Business Administration reduces risk and enables easier access to capital by working with lenders to provide loans to small businesses. The DOE Loan Programs Office administers three distinct loan programs that provide first-of-a-kind projects with access to debt capital that is not available from private lenders, with flexible, custom financing.[107]

In addition to directly supporting and fostering collaborations, start-ups and early-stage businesses must have the opportunity to contribute to setting international technical standards. By participating in international standards-setting activities organized through professional societies or industry associations, the United States can shape global technology development and support access to future international markets. Standards-setting activities can take several years of deliberation and prototyping before reaching consensus. As encouraged by the National Standards Strategy for Critical and Emerging Technology,[108] new mechanisms to support participation in the development of standards activities would enable much-needed participation by small businesses pursuing emerging technologies that have not yet established a commercial market. Pursuant to this strategy, in September 2023 the NIST CHIPS R&D Office and a host of other U.S. government programs, standards developing organizations (SDOs), and industry associations collaborated to organize the CHIPS R&D Standards Summit. The event brought together CHIPS for America leaders, SDOs, and industry alliances in the semiconductor domain to prioritize semiconductor and microelectronics standards activities; foster collaboration, coordination, and innovation within the semiconductor industry's standards community; and help identify opportunities for standards innovation, and for enabling a diverse standards-capable workforce.[109]

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[103] *AFVentures FY18–FY20 Impact Report*, 2021, https://www.globalsecurity.org/military/library/report/2021/af-ventures-annual-report_20210324.pdf

[104] https://www.iqt.org/

[105] https://drive.hhs.gov/ventures.html

[106] For a comparison of models, see: Institute for Defense Analysis, 2021, *Lessons Learned from Public-Private Partnerships (PPPs) and Options to Establish a New Microelectronics PPP*, https://www.ida.org/research-and-publications/publications/all/l/le/lessons-learned-from-ppps-and-options-to-establish-a-new-microelectronics-ppp.

[107] https://www.energy.gov/lpo/loan-programs-office

[108] https://www.whitehouse.gov/wp-content/uploads/2023/05/US-Gov-National-Standards-Strategy-2023.pdf

[109] https://www.nist.gov/news-events/events/2023/09/chips-rd-standards-summit

## Advancing Research and Development to Support Manufacturing and Supply Chain Security

At the heart of the CHIPS Acts is the establishment of a robust domestic semiconductor manufacturing industry and resilient and secure semiconductor supply chain. Additionally, existing programs such as DOD's Trusted and Assured Microelectronics (T&AM) Program drive modernization of defense systems through access to advanced microelectronics technologies that leverage state-of-the-art (SOTA), commercially driven capabilities. The T&AM Program identifies and works to mitigate persistent threats throughout the microelectronics supply chain. The T&AM Program consists of the following technical execution areas: access to advanced packaging and test, SOTA microelectronics, radiation-hardened microelectronics, and SOTA radiofrequency/optoelectronics microelectronics; as well as education and workforce development, and microelectronics assurance.[110]

Opportunities for research and development to support manufacturing and to transition new technologies into production are presented throughout this report. In addition to international collaboration to diversify the supply chain, research and development efforts can help provide alternatives and substitutions for critical minerals, materials, or other key supply chain challenges. Continued analysis and monitoring of the semiconductor supply chain will inform these R&D efforts.

## International Collaboration and the Role of Trade and Diplomacy

The semiconductor supply chain is global in nature, as is the microelectronics innovation ecosystem, with research facilities and talent located all over the world. The goals and objectives presented in this strategy have been developed, and need to be addressed, in this broader context. It will be critical to leverage resources and efforts supported by allies and partners, promote opportunities for talent flow and research collaboration, ensure secure supply chains, and promote legal and regulatory frameworks that protect research, technology, and intellectual property.

The largest source of semiconductor research and development funding comes from U.S.-based private companies. The U.S. semiconductor industry has consistently invested roughly 20% of its annual revenue into R&D, the largest share of any other country's semiconductor industry. In 2021, this amounted to just over $50 billion being allocated for R&D in a single year.[111] That same year, around 80% of all global sales of semiconductors came from outside the Americas. U.S. companies therefore depend on maintaining access to sales in foreign markets to continue driving the innovation that makes them global leaders. A trade policy aimed at combatting other governments' unfair trade practices, complementing domestic policies supporting U.S. manufacturing, and working to level the playing field for technology exports, is essential to maintaining U.S. leadership in microelectronics.

U.S. government agencies, including the Department of Commerce and the Office of the United States Trade Representative, are undertaking efforts to ensure that all governments commit to facilitating the sound development of the semiconductor industry through market-based principles, and that competitiveness of companies and their products is the principal driver of innovation, industrial success, and international trade. DOC is also working with partners and allies to strengthen companies' semiconductor supply chains in the United States and in like-minded economies to build resiliency and incorporate national security priorities to strengthen global supply chains.

Technology diplomacy is an important tool for expanding cooperation with and among allies and partners. The use of targeted dialogues, task forces, memorandums of understanding, science and

[110] https://www.cto.mil/tam/

[111] https://www.semiconductors.org/resources/2022-state-of-the-u-s-semiconductor-industry/

technology agreements, and other focused efforts on microelectronics can help strengthen bilateral and multilateral collaboration. Furthermore, several agencies have efforts to support international R&D collaboration that can be used to advance specific research goals, provide access to research infrastructure, and facilitate technical exchange. Greater communication and collaboration among U.S. and international researchers, industry, and end-user stakeholders to support development and maturation of novel technologies and techniques help strengthen the entire microelectronics innovation ecosystem.

As called for in the CHIPS for America Act, the State Department established the International Technology Security and Innovation (ITSI)[112] fund to promote the development and adoption of secure and trustworthy telecommunications networks and ensure semiconductor supply chain security and diversification. Strengthening the world's long-term economic security hinges on the ability support innovation that will drive the next generation of semiconductor technologies. To ensure a more diverse, resilient, and secure global semiconductor supply chain needed for advanced semiconductor development, ITSI funding will support efforts to secure critical mineral inputs, strengthen international policy coordination on issues such as research security and intellectual property protections, expand and diversify production capacity in all segments of the industry around the globe, and protect national security.

***Examples of ITSI fund activities***

***Ecosystem Reviews:*** *In 2023, the U.S. State Department identified five target nations ripe to expand capacity in line with the U.S. microelectronics strategy—Costa Rica, Panama, Vietnam, Philippines, and Indonesia. ITSI is collaborating with the Organisation for Economic Co-operation and Development (OECD) to conduct independent ecosystem reviews in these countries to provide a roadmap for capacity-building in the assembly, testing, and packaging (ATP) subsector. The reviews examine economic factors such as workforce development needs, infrastructure, industry-specific laws, existing technology hubs and industry strengths, and economic and policy incentives to motivate private sector investment in ATP capacity. ITSI's capacity-building programs in these countries will focus on workforce development that attracts private investment, closing regulatory gaps, and increasing physical and intellectual property protections at semiconductor facilities.*

***APEP Symposium:*** *ITSI supports multilateral partnerships to meet strategic goals, such as the American Partnership for Economic Prosperity (APEP) Semiconductor Workforce Symposium: Building Technical Capacity for a Skilled 21st Century Workforce. The Symposium will create and expand educational programs to help meet semiconductor workforce needs by building linkages between industry and technical institutions across Latin America.*

International researchers are critical to U.S. leadership in advanced semiconductors. As federal agencies develop programs and venues to enhance collaboration, considerations will be made to facilitate engagement of international researchers at the undergraduate, graduate, and professional levels with the U.S. domestic ecosystem. Enhancements to appropriate, efficient legal processes for international researchers working or visiting the United State on technical exchanges will be required. These efforts need to improve processes for accepting researchers on various U.S. nonimmigrant visas, including but not limited to F-1s, H-1Bs, and J-1s or employment-based immigrant visa categories that include students, researchers, and experts.

Another opportunity for international collaboration is in the area of education and workforce development. Semiconductor companies have facilities all over the globe, and there are several models

[112] https://www.state.gov/the-u-s-department-of-state-international-technology-security-and-innovation-fund/

for successful training programs. Development of skills and technical capabilities for specific job categories can help address skilled workforce shortages. Building partnerships between education institutions and sharing curriculum and training resources can help address the need for a well-prepared workforce and promote worker mobility.

Start-ups and small businesses around the world are also innovating in semiconductors and related technologies. Existing mechanisms such as the Quad's Technology, Business, and Investment Forum[113] and new mechanisms can be used to connect with start-up and innovation ecosystems around the world. Federal agencies can continue to facilitate bilateral and multilateral dialogues and opportunities for U.S. industry and investors that highlight promising technologies and entrepreneurs to expand the U.S. innovation ecosystem.

## Future Directions

The CHIPS Act investments present a unique opportunity to not only incentivize domestic semiconductor manufacturing, but also to strengthen the microelectronics R&D ecosystem to advance America's competitive position for the future. The semiconductor industry is rapidly evolving as these historic programs are being implemented, and business as usual will not be sufficient for success. Agencies must work together, along with academia, industry, and international allies and partners, more closely than ever before to ensure that CHIPS investments build a vibrant ecosystem that fuels future innovations. The U.S. government R&D microelectronics portfolio spans the full range—from early-stage fundamental research through manufacturing processes—and while each program has a specific role, the broad array of programs needs to be carefully connected to facilitate pathways for new research advances to be translated into commercial applications.

The CHIPS for America Act directs the Subcommittee for Microelectronics Leadership to "coordinate microelectronics related research, development, manufacturing, and supply chain security activities and budgets of federal agencies and ensure such activities are consistent with" the strategy presented in this document. To better understand the whole-of-government efforts that support microelectronics R&D, the SML will conduct a portfolio review of federal investments and cross-walk these investments against the priorities identified in this strategy within 180 days of publication, and annually thereafter. This review will provide agencies with better visibility into one another's programs and priorities and inform annual budget preparation. Given the extremely dynamic nature of the industry and the series of profound shifts in technology that are occurring, it is essential that the strategy remains agile and responsive to the changing environment. While this strategy document is a starting point, the annual reviews will provide an opportunity for the agencies to continually realign and focus their efforts to maintain progress. The SML will play a critical role as the forum for interagency coordination in the coming months and years as new programs are established, and will ensure that investments made by individual departments and agencies are synergistic and fully leveraged, avoiding both duplication and gaps.

The success of this strategy, and the CHIPS Acts more broadly, depends heavily on addressing the significant workforce needs. The SML Education and Workforce Interagency Working Group will coordinate interagency efforts across the educational spectrum and work closely with new entities that may be established, such as dedicated centers of excellence. International diplomacy and trade play important roles in ongoing efforts to regain U.S. leadership in semiconductor manufacturing and to ensure supply chain security. As noted throughout this document, engagement with allies and partners will be critical to advancing the goals of this strategy, and the SML International Working Group is an

[113] https://www.whitehouse.gov/briefing-room/statements-releases/2023/05/20/quad-leaders-summit-fact-sheet/

especially important forum for interagency collaboration as key CHIPS provisions are implemented. Engaging with leading experts around the world will help advance the frontiers of microelectronics research, support mutually beneficial intellectual partnerships, build networks that link expertise and leverage investments, and promote access to unique research infrastructure that enables new innovations.

As the birthplace of the microelectronics revolution, the United States has led the world in the development and application of semiconductor technology, technology that now underpins every aspect of our economy and security. However, international competition is intense, and continued leadership is not guaranteed. The historic investments in the CHIPS Acts provide both an exciting opportunity to revitalize the domestic microelectronics R&D ecosystem and a daunting responsibility to ensure that those investments guarantee the nation's long-term national and economic security. The United States is at its most powerful when Americans bring their diverse expertise, entrepreneurial spirit, and drive to focus on a common purpose. This strategy provides a framework to create that focus, not only to guide the U.S. government's efforts, but to convene the entire microelectronics R&D community—innovators, educators, allies and partners, and policymakers—to bring into being the technologies required to realize America's immense aspirations.[114]

[114] https://www.whitehouse.gov/ostp/news-updates/2023/03/03/remarks-of-ostp-director-arati-prabhakar-at-the-2023-aaas-annual-meeting/; https://www.whitehouse.gov/ostp/news-updates/2023/03/13/remarks-of-ostp-director-arati-prabhakar-at-an-event-on-president-bidens-fy24-budget/